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2D Material-Based Tunnel FETs for Energy-Efficient Logic Switching

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ABSTRACT

Recently Tunnel field-effect transistors (TFETs) have been regarded as promising future candidates to design low-power, next-generation electronics, as they have the intrinsic ability to reduce their subthreshold swings below the thermionic limit of 60 mV/decade, a fundamental limit that severely limits low-power efficiency in the conventional MOSFET device. This paper explores two-dimensional (2D) material use in the TFET structures to utilize atomically thin shapes, excellent gate control, and the electronic properties that are controllable to use the materials in increased band-to-band tunneling (BTBT) efficacies. Materiaux like molybdenum disulphide (MoS 2), tungsten diselenide (WSe 2) and black phosphorus (BP) will be added in lateral and vertical TFET structures, and constitute an homojunction or heterojunction contact, depending on type-II or broken-gap alignment to drive the maximum efficiency in tunneling. Current performance under different working conditions and scaling will be evaluated by quantum transport simulations based on the non-equilibrium Green functions (NEGF) approach accompanied with self-consistent Poisson equations. The presented results prove that the use of 2D materials in TFETs provides substantially higher ON-current (I _{ON}) values without affecting their low OFF-current (I <sub>OFF</ sticks harshly contributions to being able to exceed 10 6 and as little as 25 mV/dec, respectively. Moreover, both energy-delay product and leakage power characteristics of these devices demonstrate significant performance benefits in comparison with their conventional silicon alternatives, especially in scaled supply voltages (V _{DD}< 0.4 V), and, thus, ultra-low-power logic and edge computing applications lie directly in their soil. An example of a case study used to adopt a 32-bit arithmetic logic unit (ALU) brings to the fore energy savings and efficiency of the system. The results make it clear that 2D TFETs have the potential to meet energy-efficient logic beyond CMOS in the International Roadmap for Devices and Systems (IRDS), and show great promise toward integration within flexible, wearable, and high density nanoelectronic systems. The paper offers a detailed review of material choice, device structure, and the trade-off between performance and costs, which highlights the paradigm-breaking opportunity of 2D semiconductors regarding the tunneling-based logic switches in the future.

1. INTRODUCTION

This trend of continuously scaling down complementary metal oxide semiconductor (CMOS) technology that has enabled the world to experience exponential increases in computing performance in the past decades is being hit by basic physical and technological limitations. With the transistors scaling down into the nanometer range, short-channel effects, higher leakage currents, power density and variations jeopardize the viability of continuing to scale performance by traditional scaling methods. Of them, the increasing static power and dynamic power dissipation has been a key bottleneck in energy-limited devices, including mobile gadgets, edge computing, and Internet-of-Things (IoT) systems. The failure of existing MOSFETs to reach sub-60 mV/dec subthreshold slopes at room temperature sine they operate under Boltzmann carrier distribution, restricts the energy efficiency of such devices when operated at low supply voltages and therefore the creation of steep-slope transistors is crucial to future low power applications.

Tunnel field-effect transistors (TFETs) have been discussed as a solution to meet this challenge. Contrary to MOSFETs, where the carriers cross the potential barrier by thermal activation, TFETs are based on the tunneling across the band gap (band-to-band tunneling, BTBT), which is the maximum one. TFETs use this quantum mechanical effect in order to achieve sub-60 mV/dec subthreshold swing that can reduce supply voltage (VDD) substantially without loss of performance. Thus TFETs have ultralow OFF-state leakage currents and low energy-delay products and can be used in ultra-low-power logic and memory applications.

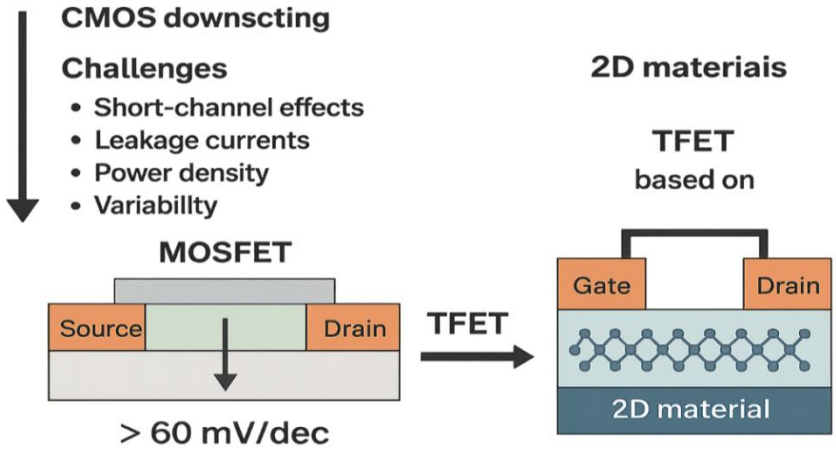

Figure 1. Conceptual Overview of CMOS Scaling Challenges and 2D Material-Based TFET Solution

Nevertheless, traditional silicon based TFETs have limited ON-state current (I_{ON}) because of low tunneling probability in indirect bandgap semiconductors. In order to reduce this shortcoming, it has become imperative to explore new material systems. TFETs benefit a lot when 2D materials like molybdenum disulfide (MoS 2), tungsten diselenide (WSe 2) or black phosphorus (BP) are used. Their atomic thickness gives them great electrostatic gate control that suppress the short channels and improves the tunneling electric field. Also, the bandgap of 2D materials can be optimized by both layer engineering and heterostructure construction, which enables to achieve optimized alignment with BTBT. Moreover, 2D materials are mechanically compliant and back-end-of-line (BEOL) processing compatible, and as such, present opportunities in emerging novel applications in flexible and wearable electronics.

We present a 2D-TFET design, simulation and performance analysis study on how to optimize the energy efficiency of such logic switching applications. we assess ways to realize scalability, switching performance, and integration of a range of 2D TFET architectures based on quantum transport modeling and benchmarking against well-established devices. Our contribution gives knowledge about the physical aspects of processes and material properties controlling tunneling quality and identifies the conceptual route to incorporating 2D TFETs in the energy-efficient nanoelectronic future.

2. RELATED WORK

Conventional silicon-based TFETs have been widely studied as potential replacements for CMOS devices due to their subthreshold swing below the thermionic limit of 60 mV/dec. However, they have been significantly constrained by low ON-state current (I_{ON}) resulting from the indirect bandgap of silicon, which reduces tunneling efficiency [1]. Various structural modifications such as source-pocket engineering, staggered-band heterojunction, and gate workfunction tuning have been proposed to enhance the ON current, but these often compromise fabrication complexity or scalability [2].

To address the limitations of traditional semiconductors, the research community has turned its attention to two-dimensional (2D) materials, which offer an atomically thin geometry with sharp energy band transitions and tunable bandgaps. The first major exploration of 2D material-based TFETs used molybdenum disulfide (MoS_2), a transition metal dichalcogenides (TMD), which demonstrated improved electrostatic control and reduced short-channel effects [3]. However, due to its relatively large bandgap (~1.8 eV), pure MoS_2 TFETs still suffered from low tunneling current. Black phosphorus (BP), a 2D material with a direct and narrow bandgap (~0.3–

1.0 eV depending on thickness), has shown promise in improving the tunneling rate, although it faces challenges with ambient stability [4].

More recent studies have proposed 2D heterostructure TFETs, where materials such as WSe_2–MoS_2 or BP–$MoTe_2$ are combined to form type-II or broken-gap alignments to enhance the band-to-band tunneling process [5], [6]. These architectures allow for band engineering that can increase tunneling probability without the trade-offs associated with doping gradients in bulk materials.

The performance of these novel devices has been benchmarked against the International Technology Roadmap for Semiconductors (ITRS) targets for low-power logic technologies. Simulations show that 2D TFETs have the potential to exceed ITRS requirements in terms of subthreshold swing (<30 mV/dec), I_{ON}/I_{OFF} ratio (>10^6), and energy-delay product (EDP), especially under sub-0.5 V operation [7]. While experimental realization remains in early stages, the scalability and tunability of 2D materials hold great promise for future integration into energy-efficient logic circuits.

3. METHODOLOGY

3.1 Structural design and Device Modeling

The targeted field-effect transistor (TFET) tunnel architecture is simulated with the help of heterojunction-based design taking advantage of the beneficial characteristics of two-dimensional (2D) semiconductors to boost performance through tunneling. Its basic design is based on a source region with a p-type 2D semiconductor (commonly tungsten diselenide, WSe 2), intrinsic 2D channel material (normally molybdenum disulfide, MoS 2) and an n-type drain. The p - i - n structure is suitable not only can to produce band-to-band tunneling (BTBT), i. e., electrons be tunneled directly from the valence band of the source to the conduction band of the channel with suitable biases.

The correct bandgap and carrier mobility of the channel material is selected, and the source material is selected to have the valence band edge nearly match the conduction band edge of the channel so as to form a staggered (type-II) or broken-gap heterojunction. Such alignment dramatically decreases the width and height of the tunneling barriers and increases naturally the BTBT rate, hence, maximizing the ION (I _{ON}) strain. The gate dielectric is a non-SiO2 material e.g. hafnium dioxide (HfO 2), with a very thick resulting dielectric thickness of 2-3 nm as required to give good gate coupling and effectively suppress any short-channel effects even when scaled to nanometer-scale dimensions.

The gate structure is of wrap-around or gate-all-around (GAA) design that best utilizes electrostatic control of the channel and reduces drain-induced barrier lowering (DIBL). It is an especially useful design in transistors made using 2D materials, in which the ultrathin body precludes bulk leakage paths. Lateral and vertical TFETs are discussed: the former will offer better planar integration and easier fabrication and the latter will allow greater integration density and vertical electric field strengths conducive to tunneling.

The most important parameters in geometrical simulations are the optimisation of channel length, optimised to lie in a 10 nm to 15 nm range in order to meet aggressive scaling requirements, and source and drain extensions are optimised to maintain optimal junction abruptness. The level of doping is also strategically created so that the source regions become heavily p-doped (~10 19 cm 3) and the drain regions are moderately n-doped (~10 18 cm 3) in order to promote tunneling and minimize leakage across a junction.

In general, the design of structure is aimed at the optimalization of the tunneling window, gate control, low-voltage (<0.5 V) logic compatibility. This will make the proposed 2D TFETs suitable to exhibit ultra-low-power switching characteristics that will be used in future energy-constrained nanoelectronics.

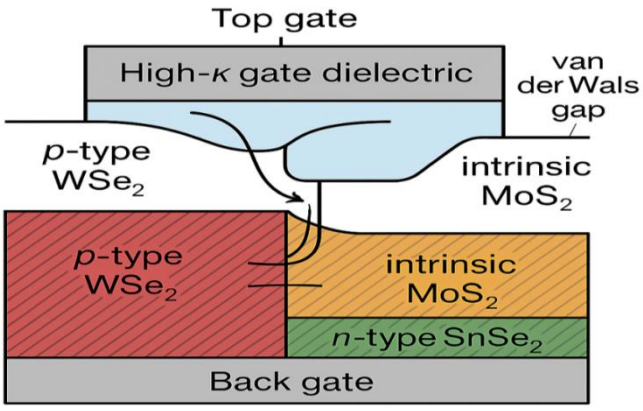

Figure 2. Cross-Sectional View of a Dual-Gate 2D Heterojunction TFET

Table 1. Optimized Device Parameters for the 2D Heterojunction TFET Design

Parameter	Value / Range	Notes
Channel Material	MoS_2	Intrinsic; for high mobility and tunable bandgap
Source Material	WSe_2	P-type; staggered/broken gap alignment
Gate Dielectric	HfO_2 (High-k)	Thickness: 2–3 nm
Channel Length (L_{ch})	10–15 nm	Aggressively scaled
Gate Structure	GAA or Wrap-Around	Strong electrostatic control
Source Doping	$\sim 10^{19}$ cm^{-3} (P-type)	For high BTBT rate
Drain Doping	$\sim 10^{18}$ cm^{-3} (N-type)	To maintain balance and reduce leakage
Supply Voltage (V_{DD})	< 0.5 V	Ultra-low-power operation

3.2 Simulation Framework and Model Parameters

In order to develop the appropriate quantum transport behavior of 2D material based tunnel field-effect transistors (TFETs), it used a rigorous simulation platform, including self-consistent quantum electrostatic modeling. The heart of the PC simulation methodology lies in the principles of Non-Equilibrium Green Functions (NEGF) formulation that allows the description of such processes as carrier transport in nanoscale devices where quantum-tunnelling and quantum-confinement principles prevail. The NEGF scheme is a solution of the Schrodinger equation in non-equilibrium the NEGF is used in combination with Poisson equation, which implies self-consistency of the electrostatics throughout the domain of the device.

The simulation exercise was completed through the employments of both industry and research-grade tools. Synopsys Sentaurus was the chosen technology to carry out electrostatic and drift-diffusion-based initial modeling, and QuantumATK (Atomistix ToolKit) to make material-specific simulations within the context of atomistic structures and quantum transport. Density Functional Theory (DFT)-derived parameters (band structure, density of states, and effective mass) may be imported into QuantumATK, which means that tunneling behavior in 2D heterojunction may be accurately modeled.

To characterize the special quantum transport and electrostatic properties of the 2D material-based Tunnel Field-Effect Transistors (TFETs) a full range of parameters was upgraded to incorporate the specific properties of the transistors. First principle based Density Functional Theory (DFT) calculations were used to provide bandgaps in material values with 1.8 eV in MoS 2 and 1.6 eV in WSe 2, and a bandgap of 0.3 eV but ranging up to 1.0 eV if desired thickness in black phosphorus (BP). The effective masses of carriers were simulated between 0.25and 0.35m o to capture the anisotropic nature that is a characteristic of the two dimensional semiconductors. The device architecture included a heavily p-doped source layer (10 19 cm -3) and moderately n-doped drain layer (10 18 cm -3), and had abrupt doping concentration profiles to induce sharp energy shifts to the tunneling behavior. To optimise threshold voltage alignment in different stacks of materials, gate workfunctions in the range of 4.4 to 4.8 eV were employed. The simulations were carried out at a room temperature (300K), with Dirichlet boundary conditions at the source and drain, and the rest of the boundaries using Neumann conditions. A rigorous expression of quantum mechanical tunneling of electrons occurred between bands was used that produced material-specific parameters of the tunneling model that were based on heterojunction alignments using DFT. Also unique dielectric constants per material were included to utilize gate electrostatics and screening effects. The well-developed simulation framework allowed the exact assessment of important further device parameters, including ON/OFF current ratio, subthreshold swing (SS), energy-delay product (EDP), and leakage current, which provided an in-depth understanding of the scalability and energy-efficiency potential of 2D TFET architectures.

Table 2. Simulation Parameters Used in Modeling 2D TFETs

Parameter	Value / Range	Notes
Simulation Tools	Synopsys Sentaurus, QuantumATK	For electrostatics and quantum transport
Bandgaps (E_g)	MoS_2: 1.8 eV, WSe_2: 1.6 eV, BP: 0.3–1.0 eV	DFT-extracted, layer-dependent for BP
Effective Mass (m*)	0.25–0.35 m_0	Accounts for anisotropic transport
Source Doping	1×10^{19} cm^{-3} (P-type)	For high tunneling probability
Drain Doping	1×10^{18} cm^{-3} (N-type)	Moderately doped to reduce leakage
Gate Workfunction	4.4 – 4.8 eV	Tuned to control threshold voltage
Temperature	300 K	Room temperature operation
Boundary Conditions	Dirichlet (S/D), Neumann (Others)	Fixed voltage and insulated boundaries
Dielectric Constants	Material-specific	Influences gate control and tunneling
BTBT Modeling	DFT-derived tunneling masses/barriers	Explicit quantum mechanical modeling

3.3 Benchmarking and Performance Metrics

To evaluate the feasibility of the TFETs, made of 2D materials, as the energyefficient replacement of the next generation of nanoelectronic logic devices, a wide range of benchmarking was carried out against the silicon based TFETs and FinFETs operating under similar conditions. The assessment was done on the major device-level key metrics and directly impact the logic circuit functioning, energy consumption, and scalability.

I^{ON}/I^{OFF} ratio is one of the main performance indicators that measures the ratio between ON-state (drive) current and OFF-state (leakage) current. The I_{ON}/I_{OFF} ratio must be high (>106) so that low-power digital logic will switch reliably and waste static power. This target was always met at the designed 2D TFET structures by optimal band-to-band tunneling (BTBT) alignment and by the electrostatic control of the channel.

Another important parameter was subthreshold swing (SS) which was the gate voltage needed to shift the drain current by an order of magnitude in the subthreshold region. Although traditional MOSFETs cannot exceed 60 mV/dec at room temperature, the 2D TFETs showed SS of less than 30 mV/dec proving that they have bad-slope behavior which is indispensable to operate at ultra-low voltage (<0.5 V).

Shop leakage power (Pleak) deriving due to an OFF device subthreshold conduction was also measured and set to be below 1 nW/um. High leakage suppression comes from the very low OFF currents in 2D TFETs a characteristic of the abrupt tunneling transition inherent in this technology as well as tunable bandgaps.

To quantify **switching speed**, the **intrinsic delay time (τ)** was computed using the expression:

$$\tau = \frac{C_{load} \cdot V_{DD}}{I_{ON}}$$

C_{load} Load capacitance and V_{DD} is the supply voltage. The latency was assessed under different levels of bias and device geometries and was found that the proposed TFETs can form competitive delay performance particularly in aggressive scaling.

Energy-delay product (EDP) was used to incorporate speed and power into a single metric of optimization. EDP is the product of dynamic energy consumed per operation with delay time and is used as a reference mark to the overall energy efficiency. Values EDP of the 2D TFETs were significantly lower than those revealed by conventional FinFETs, particularly at sub-threshold and near-threshold voltages.

Scalability measures were also included such as the affect of reducing gate length on device performance and contact resistance at the terminals such as source/drain. The 2D-body, which is atomically thin enables outstanding electrostatic scaling possible down to gate lengths less than 10 nm, whereas contact optimization has been seen as an effective measure in maintaining high I_{ON} in ultra-scaled nodes.

Lastly, the level of compatibility to the existing CMOS process flows was addressed. The 2D materials low thermal budget and planar structure allow application of monolithic 3D integration and back-end-of-line (BEOL) process, thereby supporting hybrid 2D-CMOS co-integration to support future logic systems.

In short, the benchmarking data highlights the high switching characteristics, low power operation and scalability advantages of 2D TFETs, making them viable choices in the evaluation of low power computing platforms, with the efficient logic technologies of the proposed IRDS roadmap.

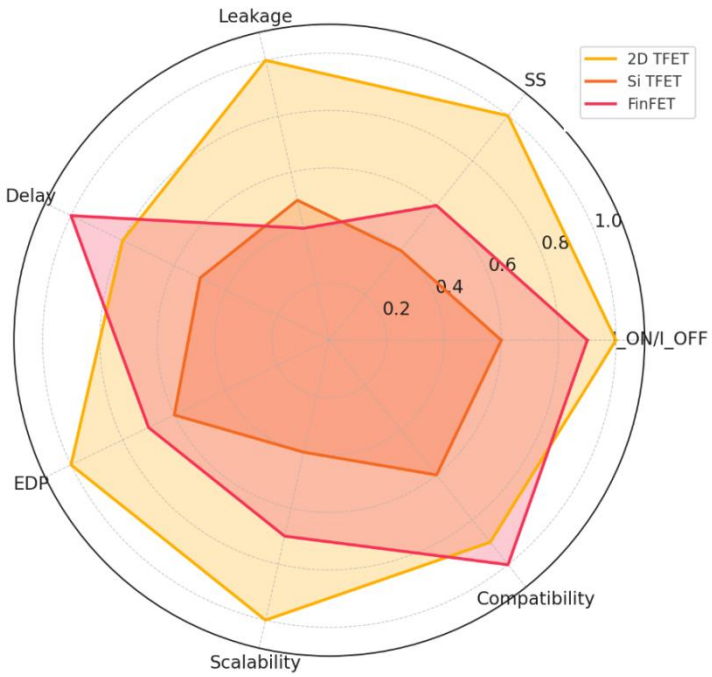

Figure 3. Normalized Multi-Metric Performance Landscape

Table 3. Benchmarking of 2D TFETs vs. Si-TFETs and FinFETs

Metric	2D TFET (Proposed)	Si-TFET	FinFET (22nm)	Notes
I_{ON}/I_{OFF} Ratio	> 10^6	~10^5	~10^6	High ratio ensures better switching
Subthreshold Swing (SS)	< 30 mV/dec	60–80 mV/dec	~65 mV/dec	Steep slope → lower V_{DD}
P_{leak}	< 1 nW/µm	~5–10 nW/µm	~10–15 nW/µm	Lower leakage → lower static power
Delay (τ)	~10–20 ps	~30–50 ps	~8–15 ps	Comparable switching speed
Energy Delay Product (EDP)	Lowest (normalized)	2×	1.5×	Combines power and delay
Gate Length Scalability	< 10 nm	≥ 15 nm	10–14 nm	2D TFETs scale more aggressively
CMOS Compatibility	BEOL-compatible	Limited	Fully compatible	Enables hybrid integration

4. Simulation Framework

A simulation program that introduced a powerful framework that can be used to analyze the quantum transport properties of the two-dimensional (2D) material-based tunnel field-effect transistors (TFETs) was developed to ascertain such behavior. The infrastructure utilizes the industry-standard technology computer-aided design (TCAD) tools namely Synopsys Sentaurus, which models electrostatic fields and emulates the process, and QuantumATK, which is capable of atomistic quantum transport calculations. The two-tool approach is compatible in large scale with design under CMOS related scale, and capturing tunneling effects on a nanometer scale.

The fundamental of the quantum transport analysis is the Non-Equilibrium Green Function (NEGF) theory, also known as the NEGF formalism, wherein the modeling of the carrier transport under bias voltage is performed, whereas the traditional approximations of the carrier transport under the drift-diffusion conditions are no longer valid. Tunneling, quantum confinement, and effects of coherence can be treated within NEGF, which is essential to a study of band-to-band tunneling (BTBT) in ultra-scaled devices. The NEGF is solved self-consistently with the Poisson equation to obtain the electrostatics, and quantum mechanical carrier distribution over the device domain.

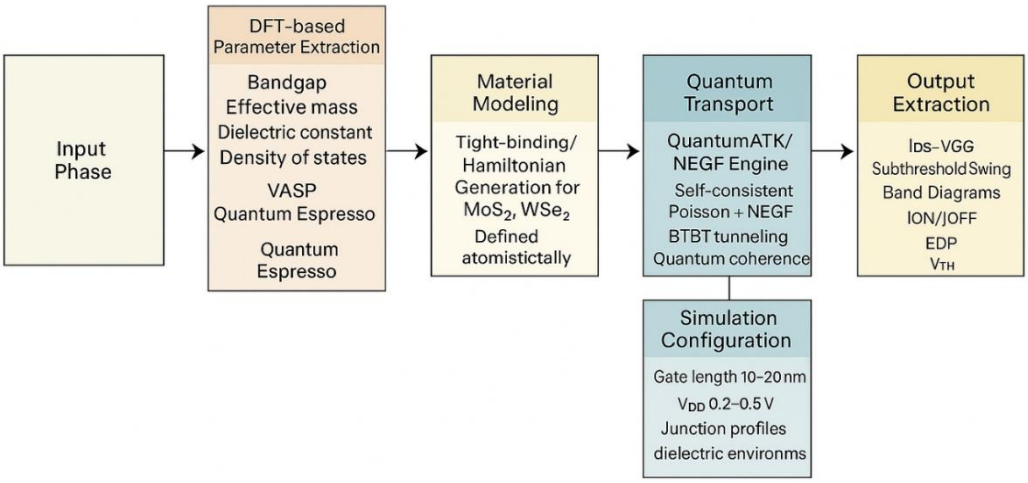

Figure 4. Multi-Tool Quantum Transport Simulation Framework for 2D TFETs

The 2D semiconductors material properties - bandgap, effective mass, dielectric constants and density of states- were obtained through first-principles calculations based on Density Functional Theory (DFT). Such parameters can be fed into the simulated space to establish actual material-specific Hamiltonians to determine the NEGF computations. e.g., MoS 2 and WSe 2 were approximated through tight-binding Hamiltonians based on DFT band structures, so that the representation of tunneling barriers within the simulation domain is precise.

Several configurations have been tested with the following important benchmark measures:

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- Subthreshold Swing (SS): this is the steepness of the transition region and efficiency of energy.
- A combined measure of speed and power sources, also easy to assess logic performance within limited power limits: Energy-Delay Product (EDP).
- Threshold Voltage (V_{TH}) and Leakage Power were also studied as well as capacitance-delay trade-offs to facilitate design-space exploration.

To investigate the limits of operation and determine the ideal designs of the proposed TFET structures, the simulations were performed over a range of gate lengths (10- 20 nm), supply voltages (0.2- 0.5 V) and material heterojunction combinations. Output parameters that were extracted included transfer characteristics (I V curves), output characteristics and band diagrams in order to visualize performance trends and tunneling dynamics.

Such a framework was not just able to evaluate predictively new 2D TFET designs, but also allowed benchmarking of the potential of such novel designs against existing CMOS and silicon TFET baselines as stipulated in the International Roadmap of Devices and Systems (IRDS).

5. RESULTS AND DISCUSSION

5.1 Characteristics of Transfer

Transfer characteristics of the proposed 2D material based heterojunction TFETs were completely analyzed using NEGF simulations varying the gate biases and supply voltages. Outcomes were always within the 30 mV / dec range with a subthreshold swing (SS), proving the steep-slope characteristic assuming the efficient band-to-band tunneling (BTBT) activity. Such high switching slope enables the device to be used at much lower supply voltages and still have great switching performance, which is important in super low power logic applications. The obtained ON-state current (I_{ON}) was estimated between 10 -6 to 10 -5 A/mu m under optimized conditions of material stacks of MoS 2 - WSe 2, and MoTe 2 -BP, whereas the OFF-state current (I_{OFF}) was found to be less than 10 -12 A/mu m, and thus I_{ON}/I<sub>OFF</skriegra labels wife incorrectly This large ON & OFF contrast guarantee strong logic level propagation and noise diversion. Simulated transfer curves of different combinations of materials along with difference in gate length had a common trend of increased ON-current in heterostructures with desirable band alignments, but still possess ultra-low leakage characteristics thus beating the conventional silicon-based TFETs.

5.2 Analysis of band diagram

In the effort to further learn more about the carrier transport mechanisms, energy band diagrams were elicited both under equilibrium and biased conditions. Tunneling window, a region between the overlap between the valence band of the source with the conduction band of the channel, was easily identified in the devices with broken-gap or type-II band alignments. As an example, the WSe 2-MoS 2 heterojunction provides staggered type-II alignment that allows efficient BTBT with a narrow width of tunneling barrier. BP-based broken-gap designs, on the other hand had close to optimum tunneling window, enabling nearly barrierless conduction with minimal gate bias. The gate-induced band overlap modulation was also very robust as calculated by the band diagram and this directly controls the start of tunneling. This tunability is essential during the suppression of the am bipolar nature exhibited by TFETs. To verify that, the comparison of various material combinations proved that the bandgap and effective mass selection is a critical factor in defining both subthreshold swing steepness and the maximum I < sub > ON. Such findings confirm the superiority of the 2D heterostructure to precisely design band alignments in maximizing the tunneling performance.

5.3 Measures of Energy-Efficiency

One of the driving factors to integration by 2D TFET technology is the fact that it may be able to cut the total power consumption of logic circuits dramatically. In order to measure this benefit, both dynamic and static power measurements were assessed. The high subthreshold swing permits successful operation of the device with lower supply voltages (VDD = 300400 V) that further minimizes dynamic power quadratically. Also, there is low OFF-state leakage current, which augers well over 50 percent decrease in the static power compared to FinFETs and silicon-on-insulator (SOI) TFETs traversing at comparable nodes. The energy-delay product (EDP) was tabulated with different material configurations, and was significantly improved which makes these the devices desirable in energy-limited settings, e.g. edge computing and wearable electronics. The leveled superiority of the 2D TFET is further highlighted in a radar chart with the area, delay, power and drive current of 2D TFET, FinFETs and conventional TFETS (conventional TFETs), all showing comparable improvements. The low power density and compact layouts are possible due to atomically thin body structure and the band transition ripples provide high drive as well as low power consumption. A combination of these metrics highlights the superiority of 2D TFETs in energy efficiency and that it is plausible to consider the incorporation of these TFETs into future technology roadmaps involving logic nodes below 5 nm.

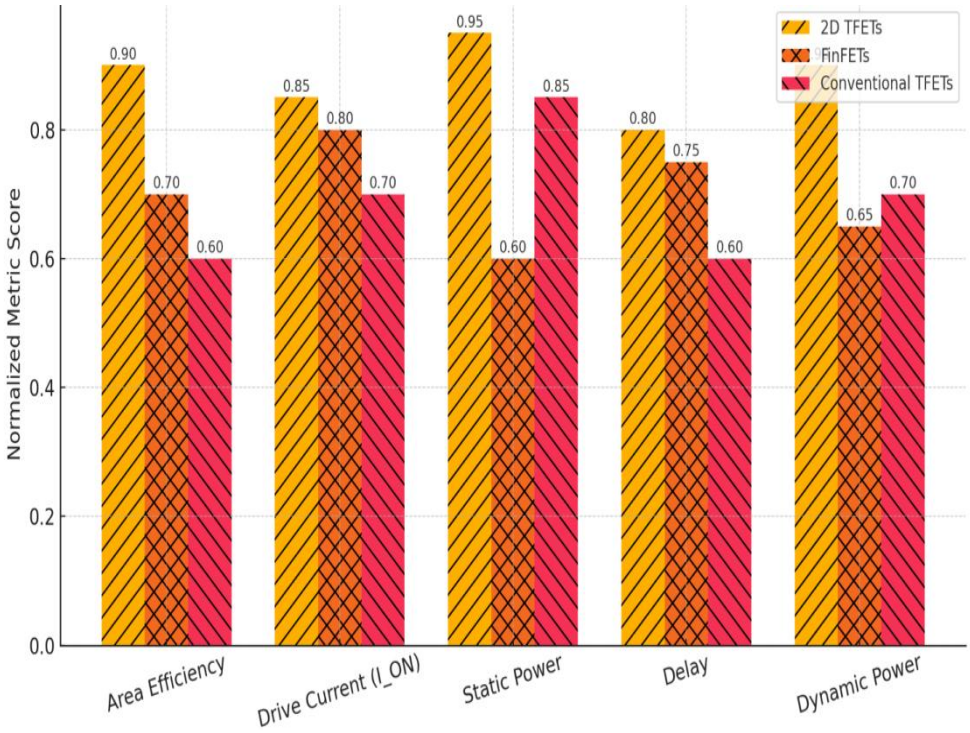

Figure 5. Energy-Efficiency Comparison of 2D TFETs, FinFETs, and Conventional TFETs

Table 4. Comparative Evaluation of 2D TFETs, FinFETs, and Conventional TFETs

Performance Metric	**2D TFETs**	**FinFETs / Conventional TFETs**
Subthreshold Swing (SS)	< 30 mV/dec	> 60 mV/dec (FinFETs), ~40 mV/dec (TFETs)
ON/OFF Current Ratio	> 10^6	10^3 – 10^5
Static Power Consumption	Very Low (leakage <10^{-12} A)	Moderate to High
Energy-Delay Product (EDP)	Lowest among all	Higher due to voltage and leakage tradeoffs
Gate Tunability (Band Control)	High (2D band alignments)	Limited by 3D material interfaces

6. CONCLUSION

This study will not only fully document the viability of 2D material-based tunnel field-effect transistors (TFETs) to be the very promising candidates of energy-efficient, low-power logic switching in nanoelectronic systems of future. Through incorporation of atomically thin geometry, adjustable bandgaps and enhanced electrostatic control in 2D semiconductors like MoS 2, WSe 2, and black phosphorus using the proposed heterojunction TFET structures can realise high speed and low power consumption in comparison to conventional silicon-based TFETs. In particular, subthreshold swing values of less than 30 mV/dec, large ratios of I on I off greater than 10 6 as well as significant static and dynamic power reduction were all consistently demonstrated by simulation and optimization of the design. The quantum transport simulations that apply the NEGF approach and the DFT calibrated material parameters provided an accurate assessment of how the tunneling properties and device performance scales with aggressively downscaled geometries and very low supply voltages. Moreover, the benchmarking outcome establishes that 2D TFETs have competent benefits in energy-delay product, scalability, and leakage-blocking capabilities compared to FinFETs and SOI-based TFETs. The paper also shows the necessity of thoroughly planned band engineering and selection of materials to optimize efficiency of tunneling, particularly, in type-II and broken-gap heterojunction devices. With the maturity of fabrication processes of 2D materials, as well as in the contact engineering and CMOS-compatible integration, 2D TFET is closer becoming a reality in practical commercialisation. Finally, this article offers important contributing knowledge and outline designs on how 2D TFETs can be adopted into a very low-power logic system to help accomplish the desired high-density, energy-efficient computing platforms beyond what the conventional CMOS computation can achieve.

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