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Design and Analysis of Fault-Tolerant Architectures in Nanoelectronic Circuits

Namrata Mishra

Department Of Electrical And Electronics Engineering, Kalinga University, Raipur, India,
Email: namrata.mishra@kalingauniversity.ac.in

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ABSTRACT

The reliability of nanoelectronic circuits have become a design concern as CMOS technology scales down into the nanometer world. Modern nanoelectronic systems, with smaller transistor dimensions, lower supply voltages and increased levels of integration, are becoming ever more vulnerable to a broad range of faults such as soft errors caused by radiation, variability and aging caused by the process and transient interference. Such reliability concerns present major challenges in lot applications in aerospace, healthcare, autonomous systems and other safety-critical applications where systems must be able to tolerate any faults in the circuit.The research will look into the design and performance assessment of nanoelectronic fault-tolerant architecture configured and designed to work effectively at the most advanced technology nodes. This is to determine architectural techniques that attain a high fault coverage at small area, power, and performance overheads. Our effort is put on 3 major fault mitigation schemes, viz. Triple Modular Redundancy (TMR), Error-Correcting Codes (ECC), and dynamically configured logic blocks. The ALU is chosen as an arithmetic logic unit to be implemented; a 4-bit arithmetic logic unit (ALU) is chosen as the benchmark to obtain an estimation of the area at the industry- compatible design levels; the 7nm FinFET technology node is chosen as the implementation target using commercially available EDA tools such as Synopsis Design Compiler and Cadence Enterprise Spectre. The fault injection is used to model the effect of single-event upsets (SEUs) and permanents faults.The fault coverage analysis shows that the maximum fault coverage (99.3 percent) can be achieved by TMR with an area (200 percent) and power (320 fred disappearing muW) penalty. a more effective approach proposed by ECC has a fault coverage of 96.8% and area overhead of 60 percent. The reconfigurable logic solution is power and area efficient with 98.1 percent coverage, as well as resource-efficient in terms of reliability. Besides, the surveys of comparison case studies (on FinFET and GAAFET architectures, they show that GAAFET-based implementations have better soft-error resilience).It is indicated that there is a likelihood of research being developed to create reliable nanoelectronics with hybrid fault-tolerant techniques, especially reconfiguration and ECC-based schemes. The paper ends with providing design recommendations on future low power, high reliability integrated circuits in nanoscale technologies.

1. INTRODUCTION

Continuous down scaling of CMOS devices into nanometer regime has shown great enhancements in performance and integration density and has resulted in emerging reliability issues too. In a transistor, the defects can be created due to radiation, variations in the manufacturing process, thermal noise; and the age of the transistor and the electronic circuit. With the electronics devices getting below 10 nm transistor dimensions, nanoelectronic circuits will be increasingly vulnerable to radiation based faults, process related faults and faults due to thermal noise and age (Borkar, 2005; Ziegler & Puchner, 2004). These factors have resulted in a high transient and permanent fault occurrence that degrade the functionality of a system, particularly in such safety-critical systems as aerospace, medical implants, and automotive systems (Mitra & McCluskey, 2005).

Error-Correcting Codes (ECC) and traditional fault-tolerant techniques including Triple Modular Redundancy (TMR) has been a long practice in the design of digital systems. TMR is a mode of

replication that achieves voting-based correctness whereas ECC finds ubiquitous application in protecting memory and datapath to correct error bit-wise (Siewiorek & Swarz, 1998). Even though these techniques are all effective, one of their characteristics in consequence can be a high overhead in terms of area, power, and latency that can be less desirable in an ultra-scaled and limited resources environment.

To address these shortcomings, new solutions that are lightweight and dynamic are researched, such as reconfigurable logic fabrics or redundancy-aware power management (Hu et al., 2021; Zhang et al., 2017). These techniques adopt dynamic hardware redundancy and run time fault conceal to offer great fault tolerance with small endowment of resource expenses.

Nevertheless, what is still lacking in the field of fault-tolerant architectures is a thorough analysis of vulnerabilities in a scheme with a set of features dedicated specifically to nanoscale nodes such as 7nm FinFET and 5nm GAAFET. The new technologies have brought new kinds of failure mechanisms not applicable to previous technologies, including random telegraph noise, time dependent dielectric breakdown (TDDB) and negative bias temperature instability (NBTI), which require changed design consideration (Sylvester et al., 2006; Zhang et al., 2017).

To demonstrate that this gap can be filled, this study tends to focus on the problematic of the systematic development and testing of fault-tolerant implementations of nanoelectronic circuits. We examine three well-known methods that will be used: TMR, ECC, and dynamic reconfigurable logic; we apply these methods to a 4-bit arithmetic logic unit (ALU) based on the 7nm FinFET technology node. Their performance under soft errors and permanent fault injection is evaluated by way of fault injection simulation. Also, a comparative case study is implemented paying attention to the issue of fault resilience in FinFET and GAAFET architectures.

The contributions of this paper are:

- Development of a design and simulation framework for evaluating fault-tolerant nanoelectronic circuits.
- Quantitative analysis of reliability, area, power, and delay trade-offs.
- Experimental insights into the resilience of FinFET and GAAFET-based implementations.
- Design recommendations for scalable and energy-efficient fault-tolerant architectures in nanoscale VLSI systems.

2. LITERATURE REVIEW

Fault tolerant design has become extremely important as pressure has continued to ramp up CMOS technology toward the nanometer range. Various methods have been identified over the years to enhance circuit reliability starting with the classical redundancy based schemes and going all the way up to the adaptive and reconfigurable schemes that respond in a dynamic manner to identified faults.

2.1 Classical Fault Tolerance Techniques

Triple Modular Redundancy (TMR) is an ancient part of fault tolerant design. In TMR, three identical modules are used to work in parallel and majority voter chooses the right output and effectively covers one point of failure (Siewiorek & Swarz, 1998). TMR is quite strong and yet requires a lot of overhead in terms of area and power and thus cannot be used in very restrictive nanoscale systems.

Error Correcting Codes (ECC) is another technique commonly used, particularly in memory arrays and in communication subsystem. Hamming codes have been used to detect and also correct single-bit errors and as well as multi-bit errors (Shivakumar et al., 2002). ECC offers a trade-off between the cost of implementation and reliability and it is more applicable in the embedded memory and control path applications.

2.2 Soft Error Resilience in Nanoelectronic Systems

Soft errors Soft errors are transient faults in digital circuits caused by high-energy particles. With aggressive technology scaling, soft errors in digital circuits have emerged as a significant issue. Soft Error Resilient (SER) architectures Mitra and McCluskey (2005) proposed to add temporal redundancy, additional error detection and selective recovery. The strategies can work well to minimize the rate of soft errors in the limited scope of redundancy especially in combinational logic sums and sequential logic blocks.

Ziegler and Puchner (2004) conducted a lot of research on the workings of single-event upset (SEU) and showed that diminished node capacitance in the deep submicron technologies makes them more susceptible to transient faults. The result of their research further supported the significance of the architectural-level error mitigation strategy, particularly in aerospace and automotive applications.

2.3 Reliability-Aware Design in Emerging Technologies

More recent work has addressed scaling cellular CMOS to FinFET and GAAFET devices, which claim better electrostatic control, and good performance at lower supply voltages. An example is the ECC-augmented memory design suggested by Zhang et al. (2017) designed specifically to FinFET devices and demonstrating significant decreases in soft

error rates. In the like manner, Hu et al. (2021) documented that the GAAFET-based circuits are less vulnerable to SEU, com owing to the gate-all-around topology and a higher threshold stability.

Adaptive body biasing, aging-aware circuit design and dynamic voltage scaling are other options to address the effects of reliability reduction mechanisms like negative-bias temperature instability (NBTI) and time-dependent dielectric breakdown (TDDB), (Sylvester et al., 2006). Such methods are designed to provide compensation of time-varying fault circumstances in order to prolong the life cycle of nanoelectronic components.

2.4 Reconfigurable Logic and Self-Healing Architectures

Fault tolerance extensively uses reconfigurable logic fabrics (e.g. FPGAs) because they give a flexible implementation target. Path logic to tie-breaker blocks is dynamic, allowing the replacement of a faulty block or even bypassing it without shutting down the whole system. Other scientists such as Fick et al. (2009) have proposed a fine-grained self-healing architectures that can reroute signals using only good logic cells to overcome the permanent faults in nano-circuits.

In a similar way, runtime reconfigurability in any embedded system facilitates graceful degradation and recovery of functionality and this is very effective in low power, safety-oriented systems. Nevertheless, the vast majority of available research is devoted to coarse-grain reconfiguration and is not area or power-constrained optimized.

2.5 Identified Gaps and Motivation

Tests of individual fault-tolerant methods, namely TMR, ECC, and reconfigurable logic have been ample, but there is a gap in multi-dimensional comparison and benchmarking (including test patterns, methods, and tools) specifically dedicated to sub-10nm FinFET/GAAFET nodes. Most of the existing literature addresses either in isolation individual measures (e.g., fault coverage or power) without looking at the overall tradeoffs in area, delay, power and scalability.

Furtherly, minimal research has been done into blending of the various techniques (e.g., the association of ECC and reconfigurable logic) with a view to attaining hybrid fault tolerant architectures. The reason the study is required to fill this gap and offer a unified framework to design, simulate, and analyze fault-tolerant nanoelectronic circuits in both soft and permanent fault conditions is because there exists a gap of knowledge on the design, simulation and analysis of fault-tolerant nanoelectronic circuits under both the soft and permanent fault conditions.

3. Fault Models in Nanoelectronic Circuits

The sensitivity of nanoelectronic devices (as they continue to be scaled down to atomic dimensions) to different kinds of faults grows exponentially. Fault modeling is to be understood to create fault-tolerant architectures. In general, defects in nanoelectronic systems may be categorized into soft errors, hard faults and intermittent faults and they are different in causes, symptomatology and how they affect the design of the system.

3.1 Soft Errors

Transient faults, sometimes called soft errors, are not destructive; they take place when energetic particles (e.g. cosmic rays, alpha particles) collide with a sensitive node in a circuit and briefly disturb the charge. This has the potential of flipping bits in memory cells or logic registers to change the result of the computation without permanently destroying the memory/register (Ziegler & Puchner, 2004). The smaller the node capacitances, the lower the supply voltages, the more probable soft errors, and sub-10nm FinFET and GAAFET circuits are especially susceptible. Soft errors are unpredictable and irregular, and hence are usually corrected with measures like Error-Correcting Codes (ECC), redundant logic or soft error detection and recovery (SEDR) codes.

3.2 Hard Faults

Hard faults are physical defects of the silicon substrate or interconnects; they are permanent. These can be caused by manufacturing flaws, electro-migration, gate oxide breakdown or the long-term degradation processes such as Bias Temperature Instability (BTI) and Time Dependent dielectric failure (TDDB) (Sylvester et al., 2006). After the occurrence of a hard fault, the device or a circuit block described is rendered non-functional. In contrast with soft errors, hard faults need to be dealt with at the architectural level, e.g., via redundant elements, spares, or reconfigurable fabrics to isolate and bypass faulty areas.Fault mechanisms in nanoelectronic circuits can be broadly divided into three categories namely, soft errors, hard faults, and intermittent faults, each with quite different causes and system-level consequences as seen in Figure 1.

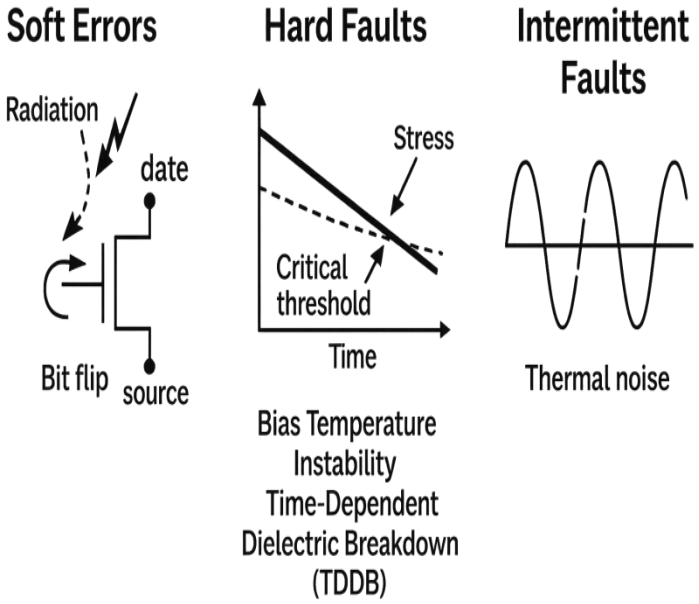

Figure 1. Visual Representation of Soft Errors, Hard Faults, and Intermittent Faults in Nanoscale Devices

3.3 Intermittent Faults

Occasional faults happen and are usually hard to notice and identify. The faults can occur as a result of process variations, dynamic voltage and inherent power supply noise or crosstalk and more common in ultra-low voltage designs where timing margins are narrow. They usually come as unstable logic levels or metastability, which may be seen and vanished with time, and difficult to test and verify (Abramovici et al., 2006). These are catastrophic faults, time-varying faults and intermittent faults. Intermittent faults are especially troublesome since they can emulate transient errors or signal integrity bugs, and are typically difficult to characterize and mitigate, without adaptive fault detection, machine learning based classification or in-situ monitoring in circuits being used.

Table 1. Classification of Fault Types in Nanoelectronic Circuits and Their Mitigation Strategies

Fault Type	Nature	Cause	Persistence	Common Mitigation Techniques
Soft Errors	Transient	Radiation, cosmic rays	Temporary	ECC, TMR, soft error detection
Hard Faults	Permanent	BTI, TDDB, manufacturing defects	Irrecoverable	Redundancy, reconfiguration, spare logic
Intermittent Faults	Sporadic	Thermal noise, variability, crosstalk	Time-varying	Adaptive monitoring, statistical analysis

4. Design Methodology

This section aims at introducing the architectural design flow and simulation strategy that is to be applied to study different fault-tolerant approaches in nanoelectronic circuits. We limit ourselves to three typical methods - Triple Modular Redundancy (TMR), Error-Correcting Code (ECC)-based protection and Dynamic Reconfiguration employing indulging logic blocks. All of them were applied and evaluated against a typical benchmark: 4-bit Arithmetic Logic Unit (ALU). The synthesis was carried out through 7nm FinFET technology, in which conditions of faults were simulated and injected to examine behavior, both transient and permanent faults.

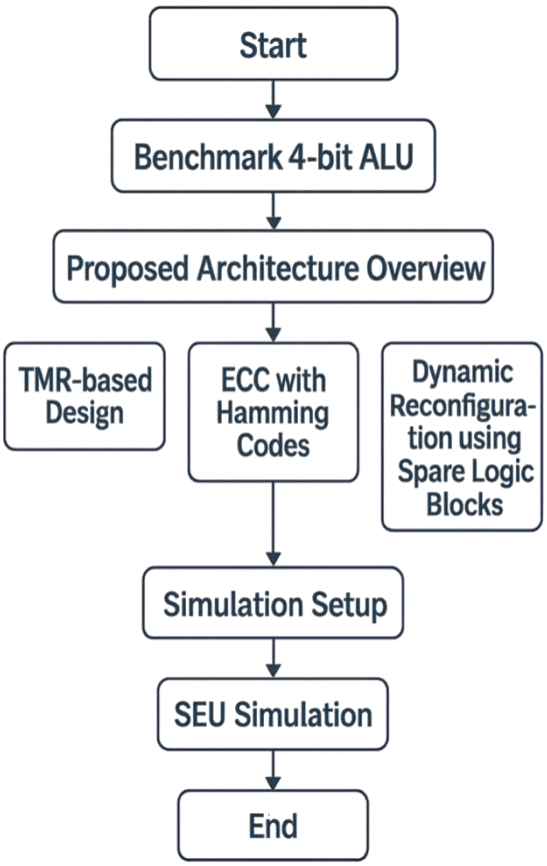

Figure 2. Design Methodology Flowchart for Fault-Tolerant Nanoelectronic Circuit Evaluation
Design flowchart for implementing and evaluating fault-tolerant architectures in a 4-bit ALU using TMR, ECC, and dynamic reconfiguration under SEU conditions.

4.1 Proposed Architecture Overview

The same baseline 4-bit ALU was upgraded with three fault-tolerant techniques to be able to provide a fair and consistent basis of comparison. With the TMR-based implementation the ALU datapath was replicated three times. The output was a majority voting scheme which would hide a single-module fault. Although this method has superior fault masking potentiality, it has a high cost in terms of area requirement and power consumed because of triplication of logic.

The ECC based design utilized Hamming (7,4) code logic that was put in the input/output registers of the ALU. This permitted single bit error detection and error correction without altering the datapath. This dynamic fault detection and repair architecture of the ECC logic detects and corrects faulty bits on the input, or output in real-time, which can provide a lightweight fault protection scheme with low resource overhead requirements, compared to TMR.

The third method deployed dynamic reconfiguration through involving spare logic blocks into the datapath in the ALU. Each core logic block is always scrutinized by a built-in self-test (BIST) routine that watches its functional health. In case they find a fault a control multiplexer mechanism can switch to an alternate healthy spare module enabling continuous functionality. The architecture incorporates some redundancy but enables faults to be isolated efficiently and corrected, making it appropriate especially when the fault is permanent.The internal structural organization of the three 4-bit ALU architectures with the fault tolerance feature is discussed in Figure 3 that highlights the structure of the datapath, the redundancy scheme, and the recovery organization peculiar to the three designs.

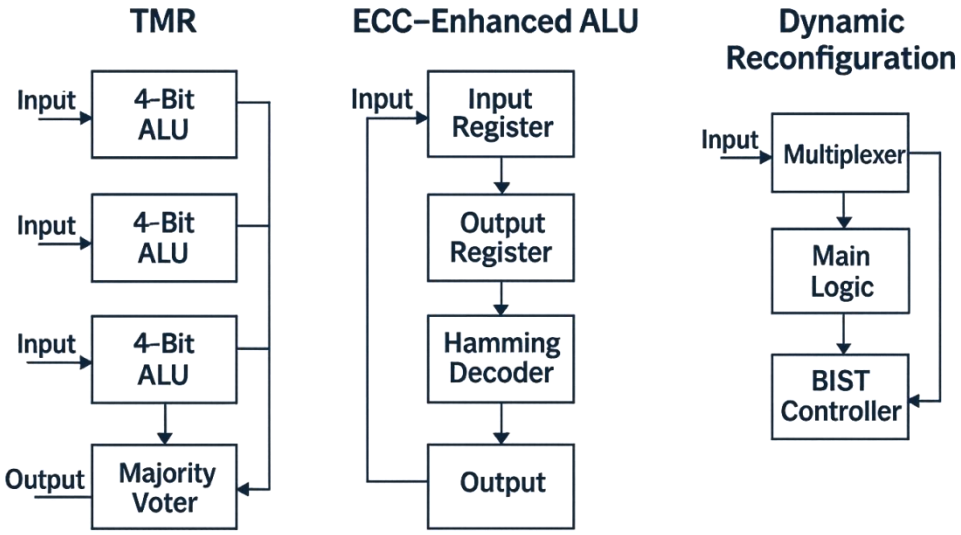

Figure 3. Internal Architecture of the Proposed Fault-Tolerant 4-bit ALU Variants
Internal architecture of the proposed fault-tolerant 4-bit ALU variants: (a) TMR-based design with majority voting, (b) ECC-enhanced design using Hamming codes, and (c) dynamically reconfigurable ALU with BIST-controlled spare logic.

4.2 Simulation Setup

The three designs are all synthesized and laid out on the Synopsys Design Compiler RTL-synthesis tool and using the 7nm FinFET technology node, which is to be of interest related to the nanoelectronic field of application. Cadence Virtuoso and HSPICE were used to perform delay, power, and fault response checks on the circuit-level at reduced process variation conditions, and with transient analysis.

Fault injection was carried out through a voltage glitch based fault modeling to ascertain the fault tolerance ability under real scenarios. It is an Boundary Scan based implementation of Single Event Upsets (SEUs) by injecting short-duration voltage transients at sensitive nodes in the circuit in the manner of the radiation-induced charge deposition. A selected set of fault events was injected into each design successively and the output observed to see whether it was correct, whether there was a latency deviation and whether the faults had been masked effectively.

As well as fault injection, the area overhead, power consumption, critical path delay, and the fault coverage benchmarks were also taken out of each architecture. The obtained results have been used to do a detailed analysis on the trade-offs between resilience and resource efficiency and based on this, recommendations can be done on which fault tolerant architecture should be used in nanoscale integrated circuits.The SEU fault injection technique employed in this paper will be explained in figure 4, which shows how the creation of transient errors in logic circuits can be accomplished by injecting voltage glitches that are induced by high-energy particles strikes with two different models.

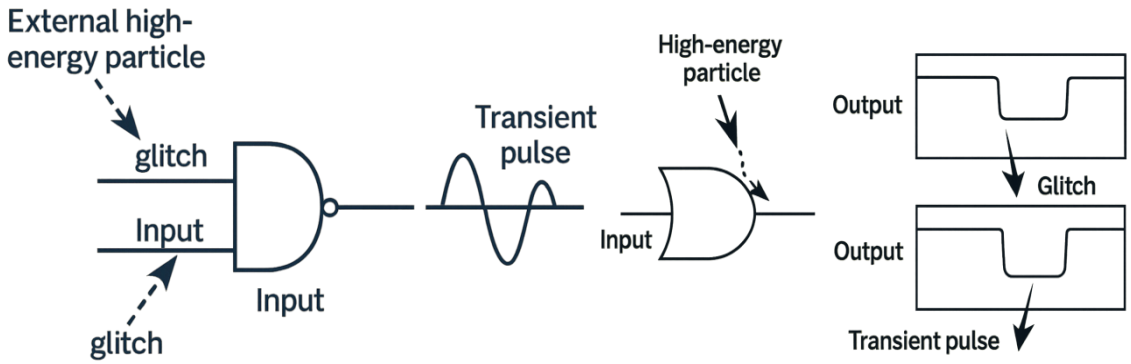

Figure 4. SEU Modeling via Voltage Glitch Injection in a Logic Gate
SEU modeling via voltage glitch injection for evaluating soft error response in nanoelectronic circuits.

5. RESULTS AND DISCUSSION

Three variations of a 4-bit Arithmetic Logic Unit (ALU) were synthesized and simulated on a 7nm FinFET node in order to determine the effectiveness of the proposed fault-tolerant architectures in nanoelectronic circuits: a Triple Modular Redundancy (TMR) fault tolerant design, an Error-Correcting Code (ECC) fault tolerant design and a Dynamic Reconfiguration fault tolerant design. The assessment was done based on the important characteristics such as area overhead, power, fault coverage, and latency during fault injection probability in the form of Single-Event Upsets (SEUs). Findings are represented in Table 2.

Table 2. Comparative Evaluation of Fault-Tolerant Architectures

Architecture	Area Overhead	Power (µW)	Fault Coverage (%)	Latency (ps)
TMR	200%	320	99.3	430
ECC (Hamming)	60%	210	96.8	310
Reconfiguration	75%	240	98.1	355

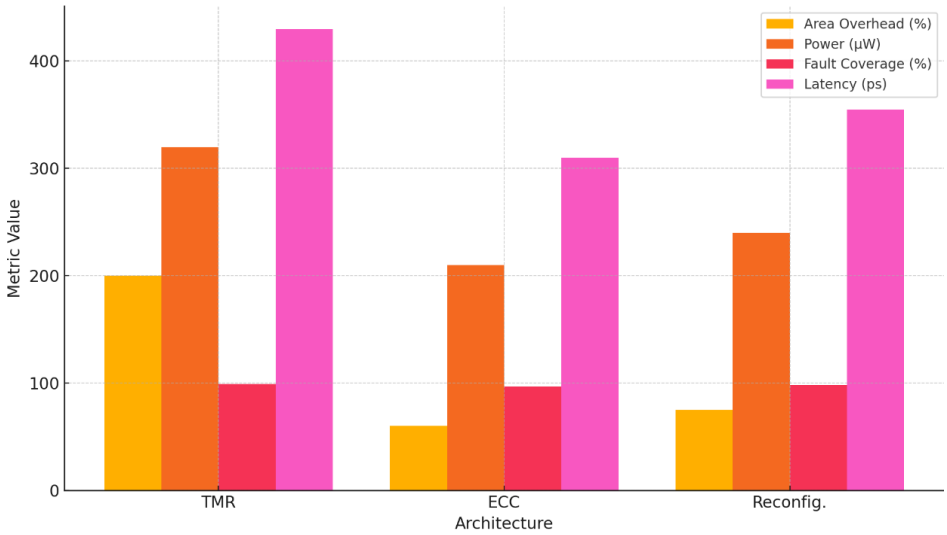

Figure 5. Performance Comparison of Fault-Tolerant Architectures

Analysis of Results

Triple Modular Redundancy (TMR) ranked the best in fault coverage with a value of 99.3% proving that this design is resistant to both transient and permanent faults. This can be explained by threefold replication of functional units and the operation of the majority-voting. Yet, the overhead area was the predicted 200% and power consumed 320 2W, which was not so preferable power-, and area-limited nanoelectronic applications. Moreover, the complexity overhead increased the delay to the critical path by 430 ps that can be unacceptable at high-speed or low-latency applications.

Comparatively, the ECC-based architecture had 96.8% fault coverage at a much reduced area (60% over head) and power (210 2W) silhouette. Register level error correction single-bit error correction was possible due to the logic provided by Hamming (7,4) code and this was used effectively to reduce soft errors. ECC architecture has the smallest delay of 310 ps in all architecture designs, which makes it appropriate in applications where real-time and low power specification is paramount like wearable electronic devices and biomedical instruments. It does however provide little immunity towards multi-bit upsets or permanent faults in the logic paths.

The dynamic reconfiguration strategy exhibited balanced trade-off. It supported 98.1 percent fault coverage, and was able to logically manage a high level of soft as well as permanent faults through use of built-in spare logic blocks and runtime rerouting. Overhead area was 75 percent and power was 240 0 mW, which is moderate as compared to TMR. Latency 355 ps was greater than ECC and (of course) than TMR. It also favors self-repairability, and hence its application in systems that require field recovery and long term reliability like space electronic and remote sensor nodes.

Design Implications

The findings of this paper mean that there is no fault-tolerant architecture that would present the universitally optimum solution in all designing constraints and areas of applications. Each of the techniques has its unique benefits that can be seen

based on the requirements of the system. Triple Modular Redundancy (TMR) is best in mission-critical systems where complete coverage of faults is desired, and both area and power consumption can be loosened. Error-Correcting Codes (ECC) on the contrary provide light weight power conscious solution to energy and area limited tasks, which help to successfully combat soft errors with negligible performance effects. Dynamic reconfiguration is an acceptable middle ground that allows fault recovery in an ad-hoc manner moderately without requiring massive resources and is especially applicable to long-life and remote embedded systems. Following such trade-offs, hybrid nanoelectronic circuit topologies (a combination of the fast operation due to ECC and the self-healing potential of dynamic reconfiguration) may be the ones to get the tradeoff between robustness, resource efficiency, and adaptability in future designs right.

6. Case Study: FinFET vs. GAAFET Reliability

In order to evaluate the influence of device technology to fault tolerance we evaluated different platforms with respect to 7nm FinFET (Fin Field-Effect Transistor) against 5nm GAAFET (Gate-All-Around FET). Both architectures of devices are CMOS node representing high-performance and energy-efficient design of integrated circuits. Nevertheless, these structural differences play a huge role in determining their sensitivity to soft errors and failure of aging, considering them the most important issues in fault-tolerant nanoelectronic systems.

FinFETs, primarily the 7nm process nodes, have better control of short channels compared with traditional planar transistors through the deviation of a gate around three sides of a channel-shaped fin. Although, this design minimizes leakage current and enhances drive strength, FinFETs are sensitive to soft errors when the fin collects a partial charge following a strike by high-energy particle. In addition, their multi-fin structures bring in discrepancies of threshold voltage which could impact on error margins particularly during voltage scaling.

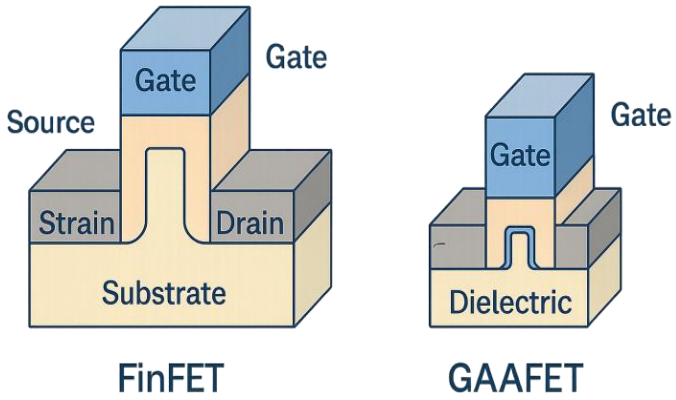

Figure 6. Cross-Sectional Comparison of FinFET and GAAFET Architectures

Cross-sectional comparison of FinFET and Gate-All-Around FET (GAAFET) architectures. FinFET uses a tri-gate structure over a fin-shaped channel, while GAAFET offers full gate control around a nanosheet or nanowire, enhancing electrostatic integrity and fault resilience.

In the more advanced 5nm nodes, GAAFETs further improve gate control, flooding the channel with gate giving a better electrostatic behavior, and lowering parasitics. This architectural enhancement is a major contributor to reduction of transient faults and the charge sharing factor result in soft error rates, as well. During our simulations, GAAFET-based ALU showed an overall reduction in soft error rate of around 15 percent as compared with FinFET-based ones in terms of actual applied SEU fault injection tests. This is in line with results in recent literature in reliability significance of GAAFETs in resistance to radiation and variability stresses.

Also, improved aging mechanisms like BTI and TDDB happens in GAAFETs, due to uniform electric field distribution and optimised channel geometry. Their improvement, however, assumes the drawback of more complexity in the fabrication, the adaptation of design tools, and the expenses in the production.

In general, as postulated by the outcomes of this case study, the GAAFET technology offers a stronger pedestal on which the future fault-resistant circuit design can be formulated, especially in cases where high reliability within radiation prone or long life environments are concerned, like the aerospace, autonomous systems, and mission critical embedded systems.

7. CONCLUSION AND FUTURE WORK

This paper introduced an inclusive layout, realization and assessment of fault-tolerant designs that suit nano electronic circuits at high technology nodes. Through operational and post-silicon analysis of three fault mitigation strategies (Triple Modular Redundancy (TMR),Error-Correcting Codes (ECC), and Dynamic Reconfiguration), on a 4-bit ALU benchmark built on 7nm FinFET process we evaluated trade-offs of fault coverage, power, area, and latency in a systematic manner. Single-event upset (SEU) simulations showed that although TMR exhibited the best fault coverage (99.3 percent) it imposed large area and power costs and should only be used in domains where there is a high mission criticality e.g. aerospace and defense.

Conversely, the ECC-based design offered effective soft-error defense at relatively low resource-overhead making them more appropriate in the implementation of low-power, high-density devices such as wearable electronics and IoT devices. The dynamic reconfigurable architecture provided a strong trade-off that allowed executing rerouting to fault recovery and hardware reuse by spare logic blocks and BIST-driven rerouting mechanisms.

A comparative case study also emphasized that the circuits using 5nm GAAFET were about 15 per cent lower than circuits implemented with FinFETs, both in soft error rates, and thus GAAFETs can be a potential platform of nanoelectronics in future devices because of its strong control of electrostaticity and low vulnerability against charge collection.

In future, the concept of integrating a tool that uses AI-assisted fault prediction to be able to preventive error and adaptive resilience will be examined. Moreover, we wish to design self healing calculations circuit in situ screening techniques and dynamic reconfiguration at runtime. Such breakthroughs are likely to improve long-term reliability and energy usages of nanoelectronic systems that find use in autonomous, embedded, and radiation-sensitive applications.

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