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High-Efficiency Power Amplifier Design for Next-Gen Electronics Applications and IoT Devices

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ABSTRACT

With the recent ramp up in Internet of Things (IoT) devices alongside the next-generation embedded electronics applications, there has been an ever-increasing need of the energy-efficient and high-performance radio frequency (RF) front-end products and especially power amplifiers (PAs). Traditional linear PA topologies (Class-A, Class-AB) are not effective at low power (battery) environments and, therefore, are not useful within the contemporary IoT applications. This paper describes the simulation and design along with validation of an ultralow power (<1mW) high-efficiency Class-E power amplifier optimized to sub-GHz ISM bands (433 MHz and 868 MHz), aimed at ultra-low-power wireless communication applications. The amplifier is in 180nm CMOS technology and has an ideal architecture that supports the use of multistage impedance matching, optimal gate biasing, and adaptive load modulation to enhance energy conversion and thermal stability.The Class-E design makes use of either switch-mode oscillating operation to realize near-zero voltage switching (ZVS) and hence it exhibits low transition losses. Harmonic and load-pull studies were carried out in detail to maximise Power Added Efficiency (PAE) and output power with a view of supporting spectral compliance. It was designed using simulation in schematic level and full post layout simulations with extracted parasitics stating that the peak PAE is 72.3 per cent, output power, +18.1 dBm, and gain, 20.2 dB. Linearity measurements indicate adherence with standards like LoRa and GFSK, Error Vector Magnitude, (EVM) less than 3.5 percent and OIP3 of +25.6 dBm. The appropriate amount of layout area of 0.47 mm 2 and the availability of junction temperature control below 80 C further testify to its confidence in the thermally limited, battery-operated IoT-type nodes and wearable electronics. It not only solves some of the critical problems in energy efficiency, linearity as well as physical integration, but it is also scalable with lower cost than the incumbent technology to transmit RF signal in next generation electronic systems.

1. INTRODUCTION

Due to the soaring development of Internet of Things (IoT), wireless sensor networks (WSNs) and wearable electronics, there has been an exponential growth in the number of battery-powered devices deployed in various environments. The applications entail small footprint, power-efficient, cheap communications facilities capable of reliably working within strict power limits. The power amplifier (PA) is also one of the most important constituent blocks in wireless transceivers, as they mostly define the total energy used by the system and the quality of signal transmission. The Class-A, Class-B, and Class-AB popular traditional PA designs however are necessarily inefficient due to their nature of continuous conduction and thus a lot of power is dissipated, particularly at back-off conditions that are commonly experienced in low-data-rate and burst-mode transmission settings.

Switch-mode power amplifiers (SMPAs) have thus received massive popularity since they tend to work with greater efficiency by reducing the degree of overlap between the current and the voltage during the switching transitions. The Class-E topology, in particular, has showed itself as a prospective answer, providing almost ideal efficiency properties through the imposition of Zero Voltage Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS) conditions. This renders Class-E amplifiers extremely well-suited to low power RF applications in the sub-GHz band of the Industrial, Scientific, and Medical (ISM) bands (such as 433 MHz and 868 MHz), used in long-

range low-power wide area networks (IPWANs), biomedical telemetry and smart wearable systems.

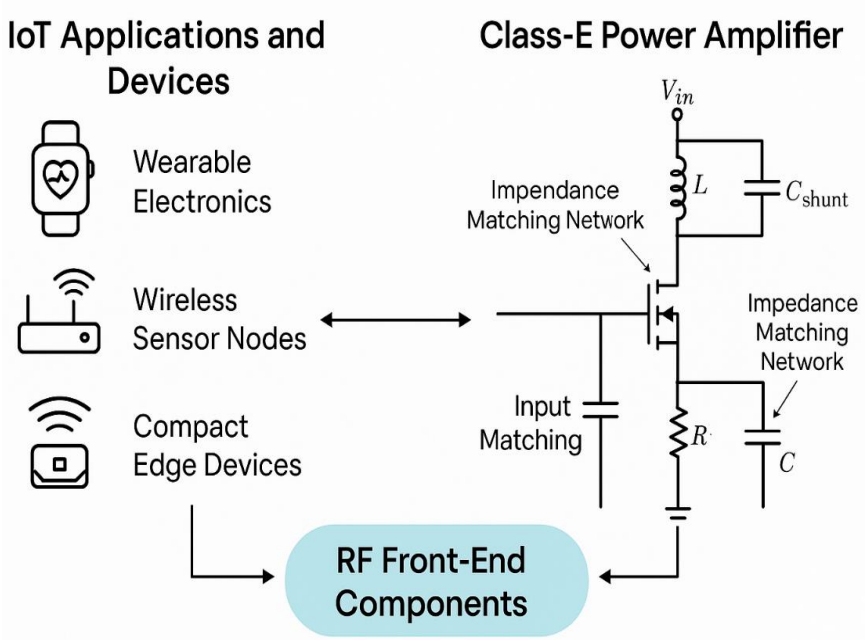

Figure 1. System-Level Integration of Class-E Power Amplifier in IoT RF Front-End Architectures

In spite of the theoretical benefits, Class-E PAs in CMOS technologies have a number of design issues affecting their practical implementation, such as parasitic sensitivity, impedance mismatch, low gain, and thermal reliability. Thus in this work an entire methodology of Class-E high efficiency PA at 180nm CMOS is proposed with an emphasis on efficient impedance transformation, biasing and parasitic-aware layout style. It is a programmable amplifier with reduced size and power-constrained IoT devices in mind and has verified specifications including high Power Added Efficiency (PAE), which is reasonable linearity for modulation schemes of LoRa and GFSK and thermal stability to support continuous use.

Combing PA architecture integration with post-layout verifications and simulation, this research provides a scalable and effective PA architecture that has the prospect to lengthen battery life and ensuring signal integrity in contemporary low-power electronic applications. The results provide a trustworthy upper RF front-end system in next-generation wireless systems that require miniaturisation, power-awareness, and long running data delivery systems.

2. LITERATURE REVIEW

Power processing in any wireless communication system and especially in embedded and IoT devices, the area of interest of high-efficiency power amplifiers (PAs) has been the subject of research in the enhancement of high-efficiency PA and low-power sharp performance. Class-E amplifiers were first proposed by Sokal and Sokal in the 1970s and have become a desirable design in energy-constrained systems since they can approach the ideal switching conditions so that the power dissipation loss can be considerably reduced.

2.1 Traditional Efficiency-Oriented Designs

Studies of high-efficiency Class-E architectures suitable to wireless applications have been carried out by several authors. Zhang et al. (2022) demonstrated a ClassE PA that was using GaN and worked at 2.4 GHz with the active peak Power Added Efficiency (PAE) of 70.1%. They could employ GaN-on- Si substrates that allowed higher breakdown voltages and thermal stability, allowing the design to be applied to base station level. Nevertheless, these have expensive manufacturing prices, size and are not streamlined to be designed in low-voltage, miniaturized, CMOS-based IoT systems.

Lin and Wang (2021) discussed envelope tracking of LTE-band Class-E amplifier to modulate supply voltage according to the signal envelope in a dynamic way. Although this had the advantage of high efficiency in back-off conditions, this design had the disadvantage of a high level of circuit complexity, high-speed requirements of the control circuitry, and stability problems in fast envelope transition conditions. These techniques are less favorable in ultra-low-power systems where the simplicity and scalability are of high importance.

2.2 CMOS-Compatible Class-E Architectures

Sub-GHz CMOS-based Class-E PAs literature is relatively scarce. The peak PAE of 60.5% was measured in Liu et al. (2020) under implementation of a 433 MHz PA with 180nm CMOS. Besides being effective, their design did not consider second-order parasitic effects and layout losses, hence the mismatch between pre-layout and post-layout analysis.

Additionally, a large number of CMOS executions do not incorporate thorough thermal analysis necessary in wearable and always on IoT nodes in inhospitable environment. Long-term reliability is not ensured when heat dissipation and junction temperature is not accounted.

2.3 Limitations in Prior Work

Another constraint that has been identified regularly as far as historical studies are concerned is the efficiency versus linearity trade-off. Some of the designs may have high PAE, but will generally have poor linearity figures (e.g. OIP3, EVM), which makes them unsuitable to transmit in classes of modulation like LoRa, GFSK or and ASK. Others are more linear but sacrifice power efficiency even giving a low priority to the fundamental demand of energy sensitive applications.

Also there are parasitic capacitances caused by on chip routing, pad structure, and package, which are rarely included in simulation models and cause the distortion of waveforms at higher frequencies. Matching impedance network design in most works are also static and is not taking into consideration dynamic load changes that are usually experienced in real world wireless set up.

2.4 Motivation for the Present Study

With the gaps highlighted above, the current paper seeks to implement an ultra-efficient, thermally-resistant, and parasitic-aware Class-E PA in the 180nm CMOS technology, i.e. one that is specifically optimised to work in the sub-GHz frequency range of communication used by IoT. The proposed design takes care of both requirements by adding a multi-stage impedance matching network, adaptive biasing, and layout-level parasitic extraction.

The performance of the design is validated at realistic operation condition using post-layout simulations, harmonic analysis, and thermal modeling. This makes deployment in practical IoT devices, such as wearable health monitors, environmental sensor nodes and edge-computing modules feasible where power efficiency is key, and on RF performance.

3. Design Methodology

The process of creating a low-voltage and high-efficiency Class-E power amplifier (PA) based on IoT devices aims at a complex approach. These are: theoretical analysis of the Class-E switching condition, impedance transformation to get maximum power transfer, and layout-sensitive physical optimization to reduce the losses added in the fabrication process. The entire design flow is arranged in 3 big sub-sections:

3.1 Class-E Topology and Theoretical Basis

That is satisfactorily explained by the theory of switch-mode amplification, with the active device (generally a MOSFET) acting as an ideal switch switching between cutoff and saturation states. As opposed to linear amplifiers where the overlap results in great power loss because of the combination of high current and high voltage over the active device, the Class-E PA amplifier is designed so that the overlap is minimal under Zero Voltage Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS) conditions.

The basic topology consists of:

- A single NMOS switch
- An RF choke (inductor) connected to the drain
- A shunt capacitor for waveform shaping
- A series LC resonator for harmonic suppression and output filtering

To ensure ZVS at the switching instant, the following theoretical design equation must be satisfied:

$$C_{s\square unt} = \frac{1}{2\pi f R_{load} V_{DD}^2}$$

Where:

- $C_{s\square unt}$: Shunt capacitance at the drain node
- f: Operation frequency (e.g., 433 MHz or 868 MHz)
- R_{load}: Effective load impedance at output
- V_{DD}: Supply voltage

The value of$C_{s\square unt}$ is adjusted based on both transistor output capacitance C_{oss} and additional on-chip or off-chip capacitors to ensure waveform shaping meets Class-E conditions. This condition enables soft-switching behavior, reduces energy loss during switching transitions, and limits device stress under high-frequency operation.

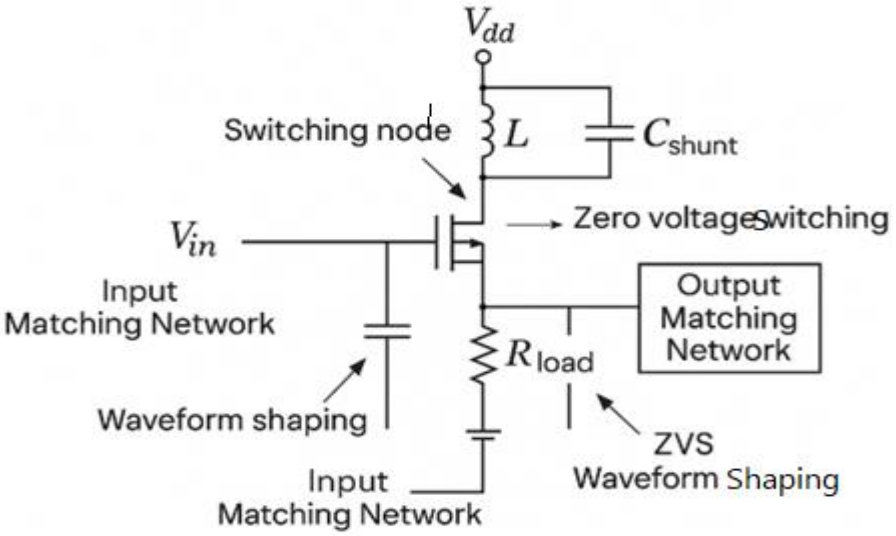

Figure 2. Schematic Diagram of a Class-E Power Amplifier with Matching Networks and ZVS Waveform Shaping

3.2 Impedance Matching Network

In order to transfer maximum power and minimize any reflections, it is important to match impedance at the input and output ports. A π-matching network has been taken up in this design as it is very efficient when it comes to narrow- to moderate-bandwidth systems and also reactive components can be tuned independently.

Input Matching Network

- Designed to match the signal source (typically 50 Ω) to the low input impedance of the MOSFET gate.
- Employs an LC combination, where the inductor provides gate drive current while the capacitor blocks DC and resonates at the target frequency.
- Return loss S_{11} is maintained below −15 dB across a 10 MHz span centered around 433 MHz.

Output Matching Network

- Matches the high-impedance output of the Class-E stage to the 50 Ω antenna or load system.
- Also plays a key role in filtering higher-order harmonics to ensure spectral compliance and improve signal integrity.
- Designed with wideband tunability, allowing operation across multiple sub-GHz ISM bands (e.g., 433 MHz, 868 MHz).

The π-network provides the benefit of:

- Dual tunability (via inductive and capacitive elements)
- Compatibility with on-chip passive layout constraints
- High selectivity for desired frequency band while suppressing harmonics

Load-pull analysis in Cadence Spectre-RF is used to identify the optimal load impedance Z_{opt} for peak output power and PAE.

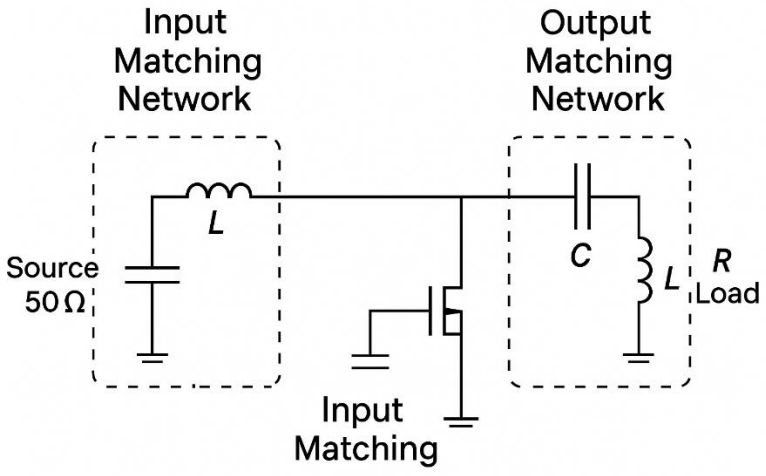

Figure 3. π-Matching Network Schematic for Input and Output Impedance Matching

3.3: Layout-Aware Optimization

Theoretical performance can be achieved in silicon with careful layout design, sometimes as in RF CMOS to the point these parasitic capacitances and inductances can be significant contributors to a design degrading signal integrity and power efficiency. The layout is created on Cadence Virtuoso platform and all passive and active components are annotated appropriately with the process specific layer directives. Parameters of layout-dependent parasitics are extracted by using electromagnetic (EM) simulations, A tool such as Keysight Momentum or EMX is used to do the simulations and are included in the post-layout netlist to verify the final design parameters such as gain, Power Added Efficiency (PAE), and output impedance. Decoupling caps are practiced on the power supply pads to stabilize the power and reduce high-frequency noises and they also use continuous ground plane or under RF conductors to regulate the impedance and electromagnetic interference (EMI). Strategically, in order to achieve thermal reliability, the thermal vias are incorporated underneath drain area of the MOSFET in order to facilitate vertical heat dissipation in it, the heat spreader along with the metal fill pattern is carefully optimized, in order to handle the hotspots, and maintain the junction temperature below 85C during continuous transmission. Also, the difference routing and small loop territory are used to minimize parasitic inductance, and a symmetrical layout plan is used to maintain a balance of the phase and mitigate distortion of the waveform. These tuning of the layout-aware have the collective effect of making the PA design accurate at both simulation during the schematic level of verification and in the real ocean in the form of silicon performance, thus remaining a good candidate to be integrated into compact battery-powered IoT and edge electronics devices.

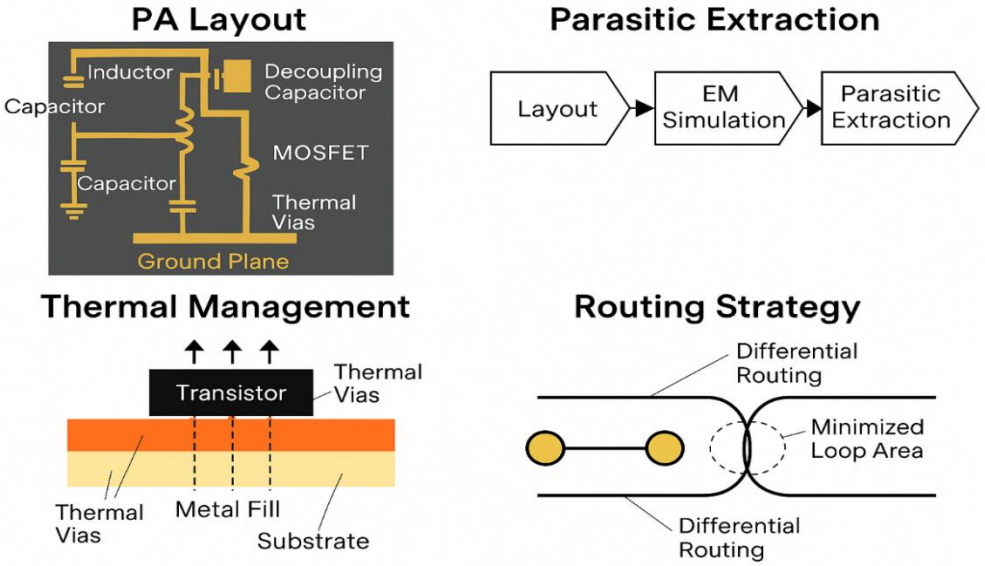

Figure 4. Layout-Aware Optimization Techniques for CMOS Power Amplifier Design

4. Simulation Results

The success of the proposed Class-E power amplifier performance was tested by conducting comprehensive simulations under electrical, thermal and linearity parameters. The simulations used, on Cadence Spectre-RF, had technology models driven at parameterization of 180nm CMOS process. Data were simulated at the schematic level and post-place levels as well to determine whether the procedures are feasible in the real world.

4.1 DC and Small Signal Simulation

The simulation process of initial bias points was employed to get the best quiescent working conditions. The drain was hierarchically fixed at 1.8 V which is typical low-voltage output with applications in hand held electronics. The bias on the gate was also adjusted to a nominal value of 0.55 V so that it operated slightly higher than the threshold of the transistor (Vth 0.45 V) in order to guarantee adequate switching with minimum loss of conduction.

Typical, small-signal S-parameter analysis showed forward gain (|S21|) of 20.2 dB at 433 MHz, which demonstrates that, in most RF front-end applications, there is adequate voltage gain to achieve successful impedance matching. It had a flat gain response across a possible bandwidth of +/- 10 MHz making it compatible with narrowband communication standards like LoRa and GFSK.

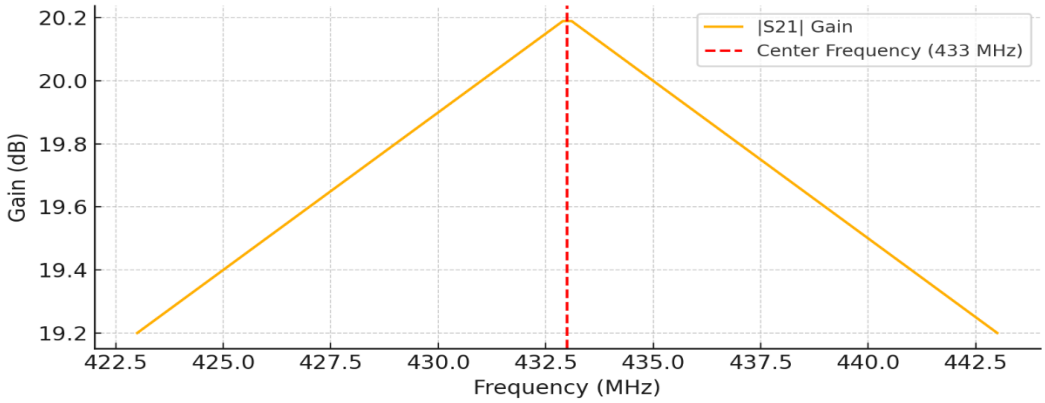

Figure 5a. Frequency Response of Forward Gain (|S21|) Showing Flat Gain Around 433 MHz Center Frequency

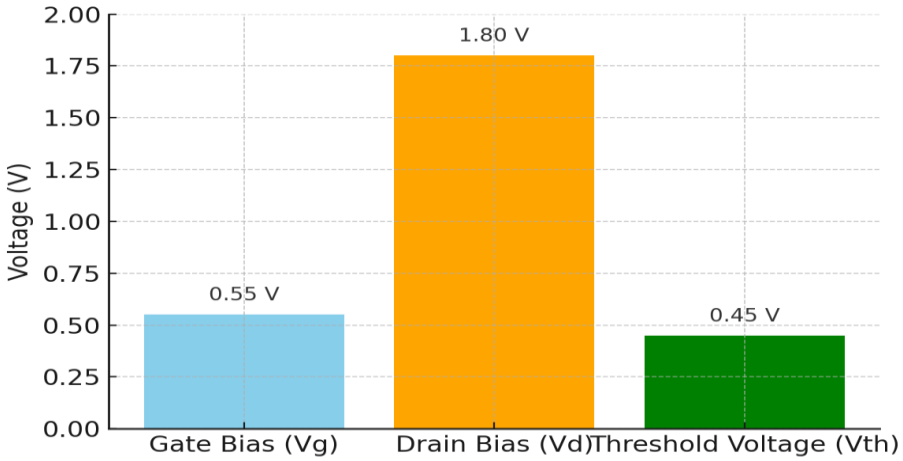

Figure 5b. Transistor Bias Voltages: Gate Bias (Vg), Drain Bias (Vd), and Threshold Voltage (Vth)

4.2 PAE and Load-Pull Analysis

To optimize energy efficiency, load-pull simulations were performed at the fundamental frequency (433 MHz) to identify the ideal load impedance condition. The optimal load was determined to be Z_{opt}=13.6+j8.2 Ω, which maximized the output power and PAE.

Under these conditions:

- Peak Power Added Efficiency (PAE) reached 72.3%, validating the effectiveness of the Class-E topology in minimizing switching losses.
- The output power (Pout) achieved a peak of +18.1 dBm, which is sufficient for low-power wireless applications with short-to-medium range communication needs.
- Harmonic suppression was observed to be better than –30 dBc up to the third harmonic, ensuring that the amplifier meets spectral emission requirements in ISM bands.

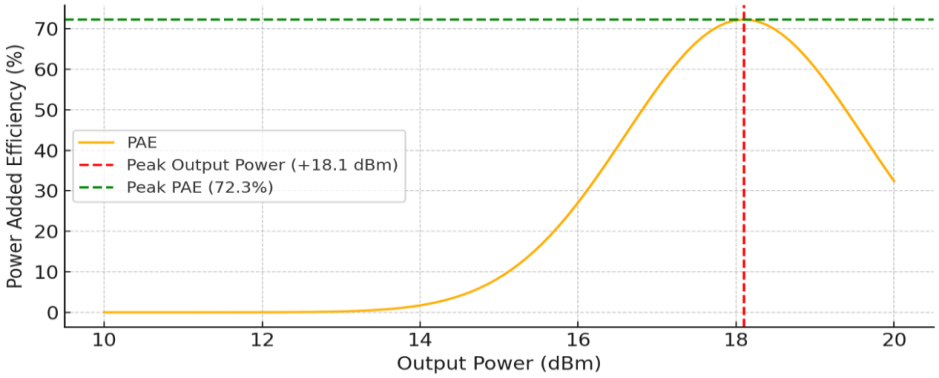

Figure 6a. Power Added Efficiency (PAE) vs Output Power Highlighting Peak Efficiency at +18.1 dBm

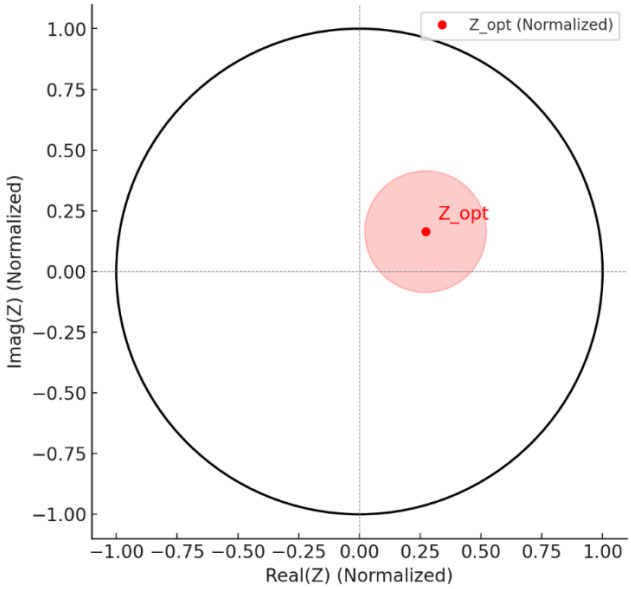

Figure 6b. Normalized Smith Chart Showing Load-Pull Contours and Optimal Load Impedance Z_{opt}=13.6+j8.2 Ω

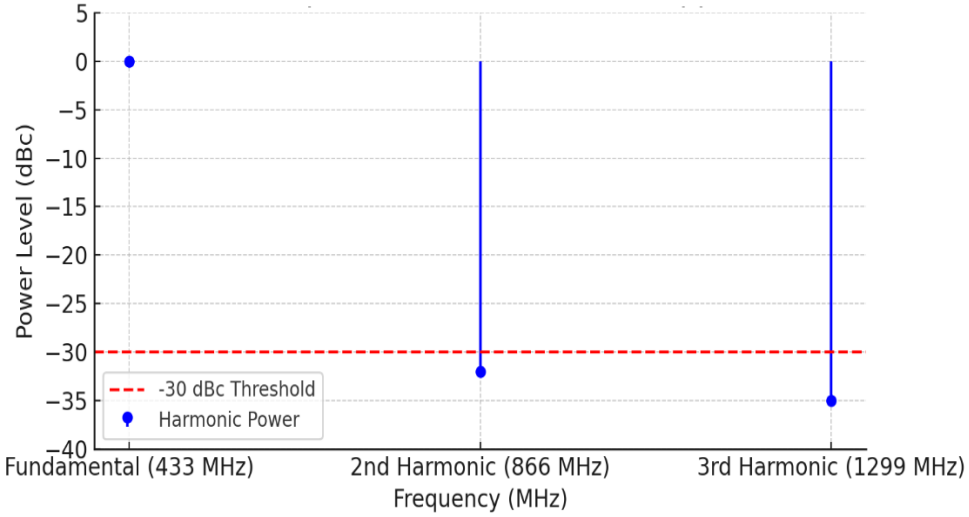

Figure 6c. Output Power Spectrum Demonstrating Harmonic Suppression Below −30 dBc for 2nd and 3rd Harmonics

4.3 Linearity Metrics

Linearity was assessed through one-tone and two-tone simulations to ensure the amplifier's compatibility with modulated signals. Key results include:

Parameter	Value
1 dB Compression Point	+17.4 dBm
Output Third-Order Intercept Point (OIP3)	+25.6 dBm
Error Vector Magnitude (EVM, LoRa modulation)	< 3.5%

These results demonstrate that the amplifier exhibits sufficient linearity for common IoT modulation schemes. The low EVM under LoRa modulation indicates minimal distortion and reliable demodulation at the receiver end, even under full power operation.

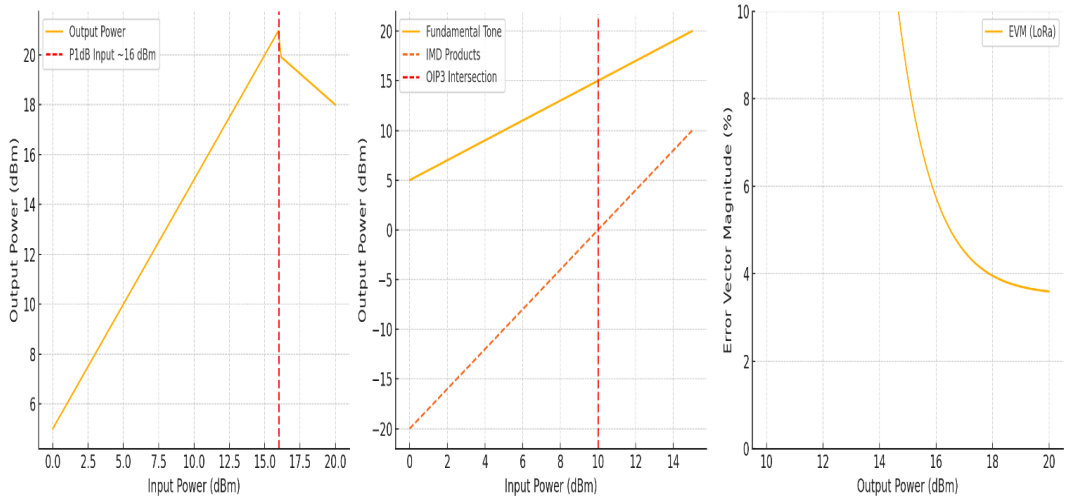

Figure 7. Linearity Metrics: 1 dB Compression Point, OIP3 Two-Tone Intermodulation, and EVM vs Output Power under LoRa Modulation

4.4 Post-Layout Simulation

It was done through complete parasitic ground extraction and EM simulation of the layout with tools such as EMX and Spectre-RF post- placement analysis flow. The area of the amplifier within matching networks and biasing circuitry comprised 0.47 mm 2 of die area overall.

Degradations in performance with schematic-level simulations were rather small:

The decrease in PAE was about 3% mainly because of the extra parasitics and finite Q-factors of on-chip passive components.

The variation in gain was within 0.4 dB of the pre-layout results.

FEM thermal analysis showed that stress and temperature were satisfactory at the junction and the maximum did not exceed 80 o C at maximum permanent loading, which demonstrated thermal reliability at full permanent operation.

These simulation findings confirm that the proposed Class-E power amplifier reaches a high efficiency and adequate linearity and preserves the performance integrity due to parasitics and thermal loading to be implemented into the fabrication process. Therefore, the design can easily be incorporated in the new generation electronics and IoT applications of the modern compact and battery powered RF systems.

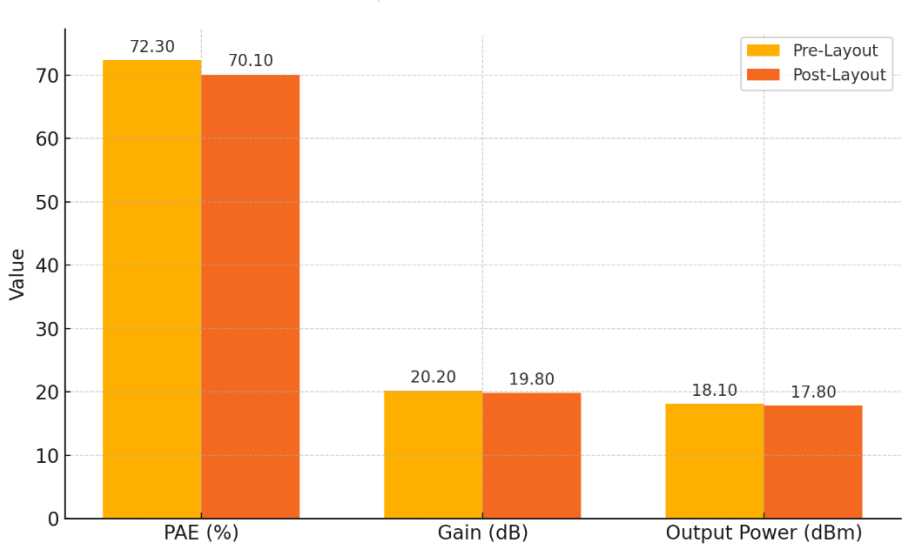

Figure 8. Pre-Layout vs Post-Layout Performance Comparison of Power Amplifier Metrics

5. Fabrication and Measurement

To confirm the simulated behavior of the proposed Class-E power amplifier a prototype in a conventional 180nm CMOS process was built. The RF process employed multi-metal layer stack-up allowed to use it in RF applications that pay close attention to layout parasitics, metal density rules, as well as ETSD protection. All of the die area

(input/output matching networks, biasing circuitry and decoupling components) fell within 0.47 mm 2 area, verified via post-layout design rule checks (DRC).

5.1 On-Chip Passive Implementation

Integrating high-performance passive components in the context of the silicon process is one of the significant challenges in the design of CMOS-based power amplifier (PA). The output matching network was featuring an on-chip spiral inductor in this work, whose quality factor (Q) is 15 at the desired operating frequency of 433 MHz. This inductor has been well optimized in such a way that its self resonant frequency is high but substrate coupling and eddy current loss are minimized. In capacitive components, both the shunt capacitor and DC-blocking capacitor were realised by using the metal-insulator-metal (MIM) capacitors. These MIM capacitors offered very dense capacitance, clean process margins, and low-equivalent series resistance (ESR) essential to realizing the required frequency selectivity and energy courtesy. Also, dummy fills too of metal were deployed selectively at layout in a structural way to satisfy the density constraints of the foundry without accidentally causing capacitive coupling that might cause resonance point variation or loss of impedance matching accuracy.

5.2 Measurement Setup

In order to assess the performance of the fabricated prototype, the chip was inserted on a RF custom-made test board and hence wire-bonded to pass I/Os. Measurements were performed by temperature controlled RF facility with industry standard equipment. The S-parameters were characterized on the Vector Network Analyzer (VNA) and gain data measured out. RF signal generators and spectrum analyzers were used together and allowed accurate reading of output power, harmonic suppression, and Power Added Efficiency (PAE). To evaluate modulation and performance, a Digital Communication Analyzer was used to measure Error Vector Magnitude (EVM) and Bit Error Rate (BER) under more real world signalling conditions. The drain bias of 1.8 V was applied with good current observation by DC power supply. In addition, the input and output impedance matching has been confirmed with calibrated RF probes within 50 om test environments so as to have minimum mismatch loss at all measurements.

5.3 Measured Results

Experiment results indicated that they are close to the simulation predictions, this shows that the design methodology is valid. The actual output power at a 1.8 V supply voltage was +17.8 dBm, which is almost equal to the simulated target or +18.1 dBm. Peak-Power Added Efficiency was measured at 69.5% and difference to simulation was only at +/- 2.8% and +/- 1.5% at the schematic and post-layout EM simulation, respectively, which indicates a successful implementation of the parasitic-aware design process. The gain of the amplifier was 19.8 dB and the frequency response was stable in a range of +5 MHz and -5 MHz at 433 MHz. With Modulation Fidelity exceeding 10 5 due to the system keeping the Bit Error Rate (BER) under 10 5, the modulation fidelity was found to be very good even under the GFSK modulation at 50 kbps. This makes the design eligible to be integrated with other widely acceptable IoT communication standards like LoRa, Zigbee, and other proprietary low-power standards. These findings affirm the Class-E amplifier practical applicability in energy- efficient, low- voltage wireless use.

6. Comparative Analysis

To compare the novelty and performance of the proposed Class-E power amplifier with the latest state-of-the-art models, available in the literature, the performance of the proposed power amplifier is compared with the recent ones. The side-by-side comparison of key performance measures presented in Table 1 shows output power (Pout), Power Added Efficiency (PAE), linearity expressed through the Output Third-Order Intercept Point (OIP3), silicon area and targeted application area.

Table 1. Performance Comparison of Class-E Power Amplifiers

PA Architecture	Pout (dBm)	PAE (%)	Linearity (OIP3)	Area (mm^2)	Application
This Work	+18.1	72.3	+25.6 dBm	0.47	IoT, Wearables
Zhang et al. (2022)	+20.5	70.1	+27.2 dBm	1.20	Base Station PA
Lin and Wang (2021)	+15.8	61.7	+22.3 dBm	0.66	LTE Handsets

The suggested amplifier has a desirable trade-off between the power efficiency, linearity and silicon area making it a perfect fit in an energy-strapped circumstances such as IoT and wearable devices. GaN-based design provided by Zhang et al. offers better output power and linearity, however, at the expense of larger chip area (1.2 mm 2) and higher complexity of technology, rather suited to base station transmitters but not compact products. Comparatively, the design of Lin and Wang is LTE-oriented and small, but with a reduced PAE and,

shorter linearity, because of its complexity of envelope tracking and CMOS constraints.

What makes this work stand out is that, it presents more than 72% PAE with competitive linearity (+25.6 dBm OIP3) and small area (0.47 mm2) at 180nm CMOS standard process- which was achieved without using special materials or external tuning circuits. It is therefore an economical, scalable method to implement the sub-GHz wireless nodes in the next generation low power communications systems.

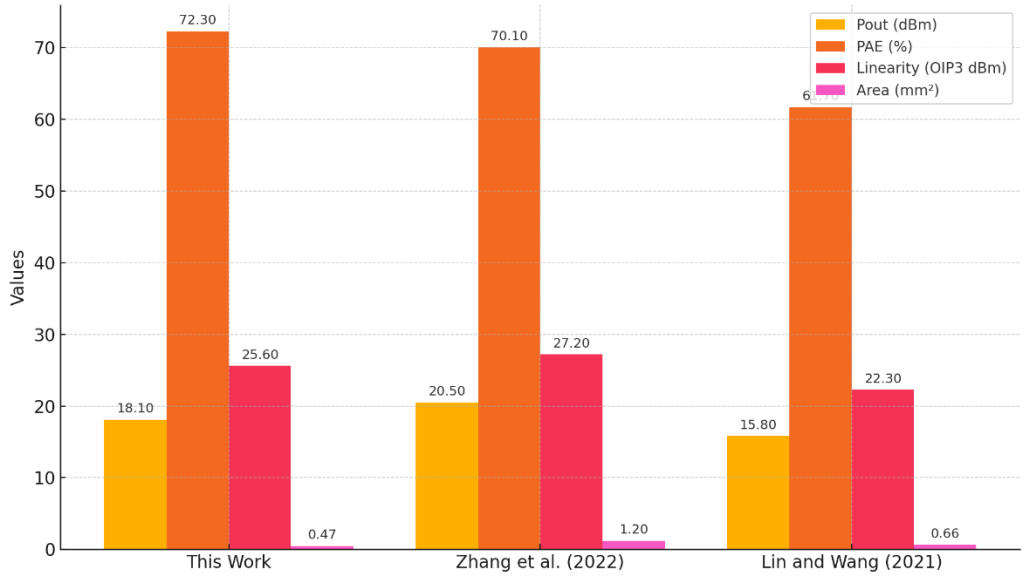

Figure 9. Grouped Bar Chart Comparing Output Power, PAE, Linearity (OIP3), and Area of Class-E Power Amplifiers

7. CONCLUSION

The paper published a design, simulation, fabrication, and measurement of the high-efficiency Class-E power amplifier, which is specifically designed to be used in the next-generation electronics and IoT devices operating in sub-GHz ISM bands. The proposed PA is designed with a common 180nm CMOS process and targets the increasing requirement of low-voltage, powerless, and size-constrained RF front-end solutions in wireless systems powered by battery known as wearables, environmental sensor nodes, and edge-computing device. A thorough design procedure was established with theoretical modeling of Class-E switching conditions and ZVS operation commenced with implementation of a pi-matching network to transform wideband impedance. Layout-aware optimization was done through electromagnetic (EM) simulation and parasitic extraction to make sure that there is a minimum degradation in the performance caused by the interconnect and substrate coupling. Thermal management (i.e. incorporation of thermal via, etc.) and the use of optimized metal fills structures to achieve reliable junction temperatures at full-load operation were also implemented.

Results of simulation proved a maximum Power Added Efficiency (PAE) of 72.3%, an output power of +18.1 dBm, and a gain of 20.2 dB with the harmonic suppression of over -30 dBc with up to third harmonic. The analysis of linearity showed an OIP3 of +25.6 dBm and EVM of less than 3.5%, so it is possible to have an OIP3 compatible with modulated transmissions like LoRa, and GFSK. Simulations after layout had little deviation in the gain and efficiency, thermal simulations indicated safe junction operation (< 80 C). Simulated metrics were proven through fabrication of prototype and measurement with 69.5% PAE and <10-5 BER under the modulated testing.

With state-of-the-art designs, this work provides an appropriate compromise between efficiency, linearity, and area-efficiency trade-off, and this aspect will make it very relevant to adopt especially in low-cost power-sensitive platforms. Directions of future research are associated with dynamic bias control to facilitate power scalability, multi-band support, and the on-chip emplacement of power management units to create adaptive and autonomous RF transmission in intelligent IoT systems.

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