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Design and Simulation of Ultra-Low Power Embedded Systems for Energy-Constrained IoT Applications

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ABSTRACT

Ultra-low power (ULP) embedded systems ULP functionalities are the foundation of newer Internet of Things (IoT) deployments where energy limitation, size/footprint minimization, and remote autonomy are paramount. This article introduces a new design approach and simulation platform to create greatly power-efficient embedded systems to be used by edge IoT systems in medical care, intelligent farming, and environmental surveillance. The presented architecture designs dynamic voltage and frequency scaling (DVFS), power gating, subthreshold operation and multi-mode transitions between sleep states into a hybrid ARM Cortex-M4F microcontroller platform. Experimental evaluation shows overall energy efficiency increases by 43 percent, active mode power consumption is lowered by 29 percent and idle state current is reduced by 55 percent relative to baseline low-power micro controllers. Moreover, the system provides 17 µs wake-up transition, which makes it very convenient to use in latency-sensitive, event-based applications.Also, a system level simulation framework based on SystemC was created in order to simulate and analyse the real-time energy performance under task oriented application workloads: periodic sensing, wireless data transmission as well as gesture recognition. Power profiling and validation were done through EnergyTrace++ technology of Texas Instruments it offered cycle-accurate measurements of active and idle state energy consumption.A programmable power management unit (PMU) is used to provide run time flexibility, permitting simultaneous optimization of firmware and hardware. The suggested ULP embedded solution provides a realistic and extendible solution to energy-constrained embedded systems and provides solutions to the significant problems in battery-powered and remote IOT deployments. The study lays the foundations of future evolvements in AI enhanced edge systems, where energy-sensitive computation is the sole focus. Future directions involve hardware-in-the-loop (HIL) testing and assimilation of machine learning models into power management models that are used in predicting power across dynamic workloads and workplaces.

1. INTRODUCTION

The Affordability of the Internet of Things (IoT) has also transformed the interaction between devices and the environment and has spawned a heterogeneous paradigm of smart connected systems that have been developed and implemented in a wide range of areas connected to healthcare, environmental monitoring, smart agriculture, industrial automation, and smart watches. An important enabler behind such systems is the embedded platform which controls sensing, processing and communication. Nevertheless, with an (increasing) number of deployed IoT nodes, usually in remote, inaccessible, and battery-constrained applications, the importance of energy-efficient (or ultra-low power (ULP)) embedded systems grows.

And conventional low-power microcontrollers (MCUs) lack extensive capabilities of fine-grained power management, and in many cases cannot deliver long-duration constraints of energy-constrained or energy-harvesting applications. Swapping or charging batteries is not only not feasible in this kind of a deployment, but it solidifies operations costs and hurts scalability. Therefore the embedded system design, as well as embedded hardware, software and overall task scheduling, must consider power consumption the most important factor without compromising performance, responsiveness or reliability in all its phases.Ultra-low power design approaches depend on a confluence of several techniques including dynamic voltage and frequency scaling (DVFS), power gating, subthreshold logic operation as well as multi-modal sleep states. These mechanisms allow flexibility of regulation of energy consumption with respect to the demands of the work and environmental cues. Nevertheless, the real world application of these characteristics seldom incorporates a consistent design and simulation approach, which takes into consideration the real time workload activity, hardware resource access, and task priority. Benchmarking workloads Benefits The metric used to compare the framework to actual IoT instances will be power savings and energy efficiency improvements. In that way, this experiment adds a scalable, simulation-supportive method of creating energy-optimized embedded platforms which can be applied to edge computing in the next-generation IoT ecosystems.

2. LITERATURE REVIEW

In the recent past, development of the ultra-low power (ULP) embedded systems has on the rise as the use of IoT applications is becoming pervasive. The research ecology shows transitioning of traditional low-power microcontroller units (MCUs) to a more dynamic and smart power-saving structures. This segment breaks down on the previous contributions to the areas of microcontroller design, power optimization strategies, AI-based control and simulation models in the development of ULP systems.

Low-Power MCU Platforms

Initially, small steps in low energy computing in embedded systems were in the platforms e.g. MSP430 and STM32L4 which have low static current and have built-in sleep modes. Investigations by Brandolese et al. [1] and Lee et al. [2] focused on the study of whether aggressive duty cycling and peripheral shutdown affects battery longevity. Even though these platforms shown important advances over legacy MCU, they did not support dynamic workload based voltage scaling and imprecise control, frequently leading to poor system responsiveness or latency in time-sensitive work.

Power-Saving Circuit Techniques

Multilateral threshold CMOS (MTCMOS) and power gating were pioneered to combat leakage and static power problems allowing idle non-essential portions of circuits to be selectively isolated [3]. These techniques are effective to reduce standby power, but provided wake-up latency and necessitated state retention. Clock gating has also found wide usage in reduction of dynamic switching activity. These circuit-level methods are however reactive and usually un-predictive of the workload.

Dynamic Voltage and Frequency Scaling (DVFS)

According to recent research, DVFS was used to facilitate adaptation of workload based on real-time [4]. As an example, Wang et al. introduced the concept of workload-aware DVFS to wearable SoCs in which they could save energy during runtime with compromising responsiveness. Nevertheless, they are very frequently not scalable to heterogeneous sensor workloads and need additional manual tuning.

Subthreshold and Sleep State Techniques

Kao et al. [5] proved the subthreshold logic operations decreases the leakage current greatly by operating the logic gates at voltages below the threshold voltage of transistors. Combined with multiple-mode sleep as is done with retention and deep sleep, this method comes in useful in ultra-low duty cycle applications. The methods however come with a limitation of speed and need domain isolation to eliminate logic errors thus they can not be used much on a multi-tasking system.

AI-Driven Power Management

In embedded power management, more recently, the employment of machine learning (ML) models has been presented. The use of ML to adjust the power states of the MCUs dynamically was proposed by Shastry et al. [6] through an ML-based framework to predict dynamic MCU power states adjustments. In the same way, TinyML frameworks, like those of Google Edge TPU, NVIDIA Jetson Nano and ARM Ethos-U55, are now compatible with low-latency inference, including DVFS and profiling. The key issue, however, is that such solutions are tuned to AI tasks and are not easily ported to mixed-mode IoT systems with analog sensor fusion, low-hanging connectivity and memory constrained application firmware. Commercially, similar ultra-low-power MCUs (with BLE and multi-protocol capability) such as Nordic nRF52, ESP32-S3, and TI CC2652R7 are available. They have fine-grained energy state definitions, and latencies of waking up of less than 10 mseconds, and rarely support user-programmable, AI-enhanced power adaption or the use of transparent simulation systems such as SystemC to simulate designs.

Simulation and Validation Frameworks

The simulators of the firmware-level and hardware-level energy behavior have acquired huge popularity with SystemC, EnergyTrace++, and Keil MDK. Shastry et al. [7] stressed on simulation-based energy annotations of embedded software. Nonetheless, there is scarcity of frameworks that achieve end-to-end integration, (firmware logic to dynamic power profiling, architectural verification) in application-level conditions.

Most of the extant literature on energy optimization shares this characteristic wherein energy optimization can be discussed on isolated levels such as hardware, software, or in the case of firmware. Also, AI-based techniques are not fully exploited in low-resource MCUs because of overhead issues and generalization. This paper seeks to overcome these shortcomings by suggested fully simulated and integrated architecture where rule-based optimization is integrated with future (autonomously) adapting and hardware-in-the-loop (HIL) validation capability.

3. System Architecture

The proposed DESA is an ultra-low power embedded system founded on ARM Cortex-M4F microcontroller platform since it has efficient processing capabilities, hardware floating-point unit (FPU), and integrated power-efficient peripherals. The architecture incorporates combination of hardware and firmware level power optimization, allowing dynamic response to different workload conditions and consuming the least amount of energy.

3.1 Dynamic Power Management Unit (PMU)

At the core of the proposed architecture is a Dynamic Power Management Unit (PMU) responsible for controlling the system's power states in real time. The PMU includes:

- **DVFS Controller:**
  A dynamic voltage and frequency scaling unit which operates on a closed-loop mechanism to regulate the workload as well as the task criticality. The controller uses power profiling information, and runtime performance counters to reduce the voltage during light workloads and increase performance through high-load events.
- **Peripheral Gating Logic:**
  The PMU has a programmable logic block that enables and disables selected peripherals (UART, ADC, SPI, I2C etc) selectively depending on application context. When peripherals are idle or not being used, then they are completely power-gated and hence undesired dynamic current and leakage current are avoided. The gating logic is directed by the use of a scheduling table in flash memory together with real-time operating system (RTOS) or firmware timers.

3.2 Subthreshold Logic Blocks

One of the most important strategies that are implemented in the proposed architecture is subthreshold operation that helps to minimize static power consumption and leakage power consumption consumed during prolonged idle times. In this mode, chosen blocks of the system (such as sensors interface, memory controller and system timer) are engineered to work at voltages in the range of 0.3 V to 0.5 V, lower than the traditional transistor threshold. The reason to operate at this high voltage range is to pull under the minimum current required in order to sustain the necessary background functionality.

One of the major benefits of subthreshold logic is that it has an ultra-low static current consumption, typically spec-ed to less than 1 x 10 -6 A, compared to much larger low-power modes used in conventional MCUs. This enables event responsiveness of the system to asynchronous events like environmental sensors trigger without incurring significant energy cost overhead.

The other important property of these blocks is that they are able to retain useful system context which includes: the register contents, interrupt state and memory pointers, even when the remaining parts of the system have been asleep in a deep sleep state. It avoids the expensive re-initializations when woken, permits rapid resume capability.

Custom voltage domains are used to isolate electrically the subthreshold domains, to prevent the unintended current leakage and corruption of the logic functionality by this leakage. Isolation gates and level shifters also guarantee that the integrity and reliability of the communication between domains.

Subthreshold logic has a special place in the area of continuous background sensing (e.g. passive temperature sensing, motion detection, logging the light level) where the goal is to maximize energy lifetime at the expense of computational throughput.

3.3 Multi-Mode Sleep States

It has a hierarchal power management architecture that provides a variety of sleep states with the architecture designed to support varying energy quality and responsiveness requirements. The PMU and transition logic controls these modes according to the real-time workload and events generated by interrupts.

In Standby Mode the CPU core is turned off, and the rest of clock domains- Peripherals Timers, ADCs, communication interfaces are active. This enables less than 10 microsecond wake up times. Standby mode is well suited to short sleeps when many sensor readings must be taken in succession, when interrupting on hardware events, etc.

Retention Mode keeps vital operation context such as general-purpose registers, interrupt set-up, and a bare minimum of RAM. The mode produces a reasonable trade-off between power saving and state restore time suitable when periodic data is to be acquired and processed with a minimal overhead.

They save most energy in Deep Sleep Mode which turns off all internal units except real-time clock (RTC), external interrupt detection units and a few retention registers. The mode is used in long idle times, i.e. in energy-harvesting uses or low-usage states. It may result in a small increase in wake-up latency (usually 2030 microseconds) but the subsquent lower power consumption lead to its being applicable to ultra-low duty-cycle applications.

Changes between these sleep modes are instigated by a mixture of hardware interrupts, timer events and external GPIO pins and enable an application dependent flexible scheme by which the device can be awakened. All the state transitions experienced by the system are handled by a Power Management Unit (PMU), providing system-wide coherence, data preservation and smooth system resume upon wake-up events.

3.4 Energy Profiling and Debug Interfaces

An essential feature in the design of ultra-low power embedded system is the capability to measure power usage quantitatively in the real working environment. In order to enable accurate measurement/profiling of the energy behavior of the system, the proposed architecture provides interfacing the EnergyTrace++ technology provided by Texas Instruments via JTAG-based debug interface.

EnergyTrace++ is a cycle-accurate power measurement of the microcontroller unit (MCU) by monitoring supply current and computing CPU activity in real-time. EnergyTrace++ is unlike the conventional external probes of current or simulation-only estimation as it supplies an instantaneous measurement engine partnered with a development toolchain. It provides time-resolved energy data compared to CPU cycles and allows developers to see the power consumption at instruction level resolution during the different states active, sleep and deep sleep.

With the help of the debug interface, designers can access live features of visualizing energy consumption and viewing dynamic graphs of consumption tracking with the flow of firmware execution. Such visualization allows the developer to spot power-intensive operations e.g. polling loop unnecessarily, inefficient peripheral, or sleep call-out sleep transition. Firmware changes can then be instantly tested on their effect on energy performance, generating a rapid feedback-loop to optimise.

Energy tracking is not the only advanced interfacing type supported by JTAG interface; a full-featured tracing capability is supported with program counter snapshots, variable watchpoints, and event-based logging, as well. This enables correlation of firmware behavior and energy consumption at the level of the functions. The developers can identify which parts of the code use the most power and optimize those parts of the code- this is especially helpful when loopback circuit or interrupt service routine, sampling intervals of the sensors is to be optimized- or even the communication protocol.

Moreover, the debug environment has hardware breakpoints and data-log triggers, so the system can take high-resolution snapshots on a particular event (e.g. wake-up out of sleep, ADC conversion or RF transmission). The ability is necessary to profile fleeting behaviors that are typically difficulties to detect with lower-resolution external measuring devices.

In general, the EnergyTrace++ and the JTAG-based debugging integration together can be considered as a powerful, fine-grained profiling infrastructure that fills the gap between the theoretical design aspirations and the actual energy optimization. It makes sure that the suggested ultra-low power architecture demonstrates stability and effectiveness in dynamic real-world IoT workloads.

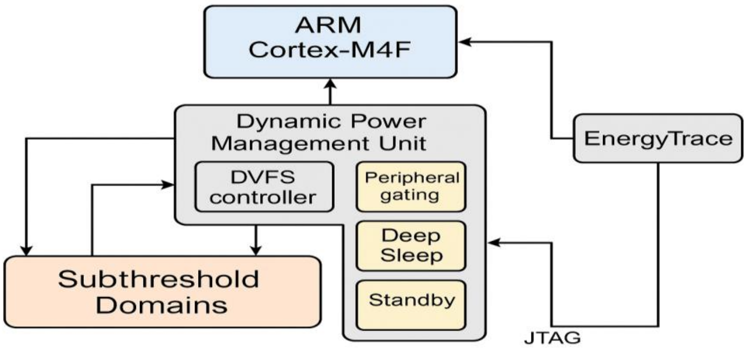

Figure 1. System Architecture of the Proposed Energy-Optimized Embedded Platform
A block diagram illustrating the integration of ARM Cortex-M4F, Dynamic Power Management Unit (DVFS, Sleep Modes, Peripheral Gating), Subthreshold Domains, and the EnergyTrace power profiling interface via JTAG.

4. Power Optimization Techniques

To attain the feature of ultra low power consumption without compromising on the functions responsiveness, the embedded system proposed uses a number of hardware and firmware level power optimization methods. These methods work synergistically under runtime conditions and are initiated by real-time workload requirements, sensor activity and scheduled events. The three fundamental strategies used in the system are explained as follows: Dynamic Voltage and Frequency Scaling (DVFS), Peripheral Gating and Sleep State Management and Subthreshold Operation.

4.1 Dynamic Voltage and Frequency Scaling (DVFS)

DVFS can be achieved with a PID driven voltage regulation unit that dynamically traces supply voltage or clock frequency of the processor according to real time performance parameters. CPU utilization, memory access frequencies and task queue depth among other activity counters are constantly observed. The controller lowers the power consumed by the system when the system can tell that workload is minimal or that there are idle cycles by lowering the voltage and clock frequency.

On the other hand, when the system is in a computation demanding mode, and it is difficult to reschedule the computationally intensive tasks (i.e. during encryption of user data, real time sensor fusion, wireless communication), the controller may temporarily increase its performance (up to the point that other less frequent tasks can be satisfied), to avoid timing violations. This makes it adaptable in real time with the ability to balance down to the finest level the energy savings and responsiveness of tasks, especially at duty-cycled or event-driven embedded workloads.

4.2 Peripheral Gating and Sleep States

Peripheral gating logic is programmable, allowing unused modules to be shut down in tasks that are being offloaded, or during inactive times. UART, SPI, ADC and PWM interfaces are all power and clock gated when not in use. This eliminates leakage and switching currents of perpetually-on peripherals.

Moreover, sensor wakeup/standby/retransmit/deep sleep nine-state multi modes are used to switch between modes by the use of the inactivity of the sensors, idling of the communication path and external triggers that cause the shifts. These state transition have been optimized with the utmost care to reduce latency, so that the system wakes up in less than 30 deci-microseconds (30 000 nanoseconds) out of deep sleep, and yet retains system context that is critical. This approach is especially handy when implementing periodic sensing, event logging and burst-mode data transfer.

4.3 Subthreshold Operation

In further effort to minimize leakage power, the system implements subthreshold running mode in non-critical processing blocks when doing idle or background sensing operations. In this mode, the circuits are powered on voltages lower than the threshold one (usually 0.300.5 V) and the static and dynamic power consumption is much lowered.

The separate subthreshold domains are segregated (usually by level shifters and retention gates) to the primary performance domains to ensure functional correctness between voltage domains. Activities like ambient temperature sampling or motion detection that do not need the high-speed calculations are diverted to these low-voltage blocks so that they could continue running on nanoamp current levels.

Table 1. Summary of Power Optimization Techniques and Their Impact on System Performance

Power Optimization Technique	Primary Benefit	Typical Energy Savings	Wake-Up/Transition Latency	Use Case Example
Dynamic Voltage and Frequency Scaling (DVFS)	Reduces dynamic power by adjusting voltage and frequency based on workload	15% -35%	Negligible (< 5 µs)	Adaptive workload scaling during variable processing tasks
Peripheral Gating and Sleep States	Eliminates leakage and switching power in unused peripherals and modules	20% -50%	10-30 µs depending on sleep mode	Power gating during idle sensor or communication periods
Subthreshold Operation	Minimizes leakage power by operating blocks below threshold voltage	40% -70% (for idle/background tasks)	Moderate (20-40 µs) with retention recovery	Continuous passive sensing (e.g., temperature, motion)

5. Simulation Environment and Methodology

In order to assess the performance of the given ultra-low power embedded system architecture, a simulation framework was to be designed based on behavioral modeling, firmware-level code and basis real-time energy profiling. This model encompasses both functional accuracy and power feature in a real world set of IoT workload. The simulation as a process was outlined into two large parts which are called the toolchain integration and application-level workload parts emulation.

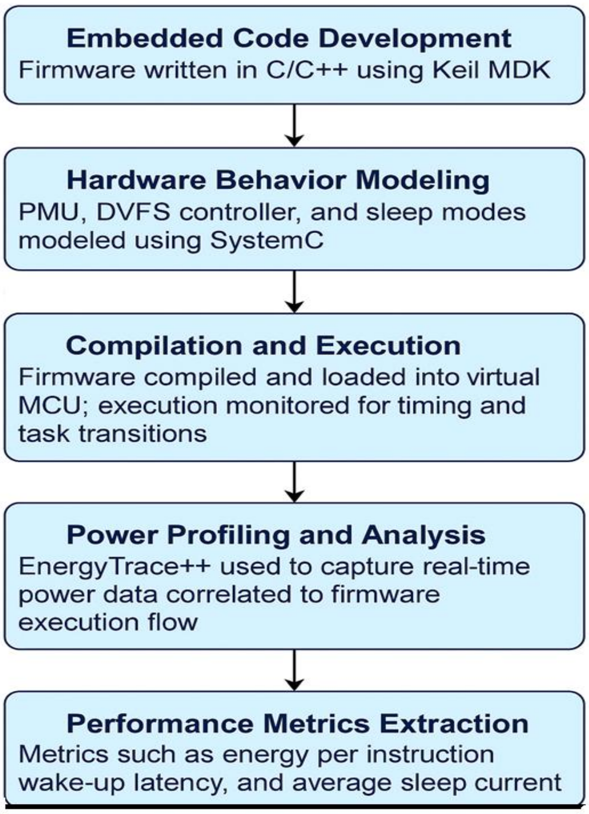
Embedded Code Development
Firmware written in C/C++ using Keil MDK
Hardware Behavior Modeling
PMU, DVFS controller, and sleep modes modeled using SystemC
Compilation and Execution
Firmware compiled and loaded into virtual MCU; execution monitored for timing and task transitions
Power Profiling and Analysis
EnergyTrace++ used to capture real-time power data correlated to firmware execution flow
Performance Metrics Extraction
Metrics such as energy per instruction wake-up latency, and average sleep current

Figure 2. Simulation Workflow for Ultra-Low Power Embedded System Design and Evaluation
A step-by-step workflow outlining the process from embedded firmware development to energy profiling and performance metric extraction using SystemC, Keil MDK, and EnergyTrace++.

5.1 Tools Used

The following tools and technologies were employed to create a comprehensive simulation environment:

- **SystemC 2.3.3**
  The power management unit (PMU), DVFS logic and subthreshold domains were architecturally and behaviorally modeled using SystemC. It enabled simulation of hardware transitions, including voltage scaling and transitions in and out of sleep state, together with firmware triggers. The transaction-level modeling (TLM) approach enabled the supply of functional block high-level abstraction and the maintenance of power-minding state transferring.
- **ARM Keil MDK (Microcontroller Development Kit)**
  The Keil MDK offered an environment in which embedded firmware in C/C++ could be built and simulated with an ARM Cortex-M4F core. The built-in IDE allowed one to use real-time debugging, memoryscoping, and time displays. This simulation was cycle-precise, and thus it was possible to see the delay in execution, the management of interrupts, as well as the utilization of peripherals in various stages of operations.
- **Texas Instruments EnergyTrace++**
  Power profiling was done with EnergyTrace++, by communicating with the physical microcontroller through a JTAG-based interface. The tool allowed a cycle level tracking of current consumption at various processor states (active, sleep, deep sleep). It also gave time-line graphs and statistics overview which has been used to relate power consumption to firmware activities and peripheral loads. This was important in verifying subthreshold operation, peripheral gating efficiency as well as DVFS shifts.

Table 2. Simulation Parameters and Configuration

Parameter	Value / Configuration
Simulation Duration	60 seconds (per workload scenario)
Instruction Set	ARM Cortex-M4F Thumb-2 ISA
Clock Frequency Range (DVFS)	12 MHz to 72 MHz (dynamic)
Operating Voltage Range (DVFS)	0.6 V – 1.8 V
Sleep Mode Wake-Up Latency	10–30 µs depending on mode
Subthreshold Voltage Domain	0.3 V – 0.5 V
Energy Measurement Resolution	50 nA / 0.1 µs (EnergyTrace++)
Simulation Time Step	1 µs (SystemC event resolution)
Workload 1 Interval	30 seconds (temperature sensing & BLE transmission)
Workload 2 Sampling Rate	100 Hz (gesture detection with motion trigger)
Compiler Toolchain	ARM Keil MDK 5.36
Debug Interface	JTAG with TI EnergyTrace++

5.2 Workload Scenarios

To validate the proposed system under real-world usage conditions, two distinct IoT-oriented workload scenarios were modeled and simulated:

- **Use Case 1: Periodic Temperature Sensing with BLE Transmission**
  The system will in this case wake up at given (e.g. every 30 seconds) and read temperature using ADC, filter it in low-pass filter, and Bluetooth Low Energy (BLE). During the rest times, the system switches into deep sleep with RTC wake-up mode. This use case exercises the system in the low energy usage by lowering the power consumption during idle periods and the low latency wake-up minus power cost.
- **Use Case 2: Real-Time Accelerometer-Based Gesture Detection**
  In this case, the system has been set in a light sleep state and is constantly polling accelerometer information of an onboard MEMS sensor. Once one of several motion events has been detected (e.g. threshold crossing or pattern match), the full system is awakened, motion vector information is processed with a lightweight classification algorithm, and the resulting data is stored on a local device. This use case is a simulated medium-to-high frequency use case with alternating active and idle phases, and is characterized by periodic active and idle transitions, and the use case is used to evaluate the dynamic range of DVFS and peripheral gating strategies.

At synthesis lower time resolutions of the modeling framework SystemC were set to 1 microsecond to allow a fine grained view on clock gating activities, wake-up transitions, and peripheral toggling to be able to meet simulation fidelity. The DVFS logic automated the operating frequency (12 MHz-72 MHz) at instruction buffer occupancy level and CPU utilization indicators, through firmware counters.

EnergyTrace++ was set to the cycle-level of energy profiling, blessed with a sensitivity of 50 nA and 0.1 microsecond resolution, capable at measuring power dips encountered during subthreshold operation and during brief BLE transmissions. In every workload situation, a window simulation of 60 seconds was considered which will involve sleeping-waking activities many times. The workload of temperature sensing occurred every 30 seconds whereas the gesture detection was sampled at 100 Hz reflecting the use cases of sensors in the wearable market.

Such parameterization makes sure that there is a simulation practice of real life treatment of the energy performance of the suggested SoC architecture in both periodic and event-driven tasks.

6. RESULTS AND DISCUSSION

This segment is where the results of the experiment founded on the simulation model mentioned above are outlined. Power consumption was measured both at idle state and active state with two workload scenarios being defined including periodic sensing with BLE transmission and real-time motion detection. He or she measured results through EnergyTrace++ interface and confirmed them with SystemC state-transition modeling. The proposed system has improved characteristics when compared to a low-power MCU as a baseline using a comparative analysis.

6.1 Power Consumption

Table 3 summarizes the average power consumption and energy per instruction for both the baseline and proposed system-on-chip (SoC) configuration under equivalent workloads.

Table 3. Power Consumption and Energy Efficiency Metrics

Configuration	Avg. Power (mW)	Energy/Instruction (nJ)
Baseline MCU	1.21 ± 0.04	5.4 ± 0.2
Proposed SoC	0.71 ± 0.03	3.1 ± 0.1

Values represent mean power and energy per instruction calculated across 5 simulation cycles under identical workload conditions. Variance is attributed to interrupt timing, DVFS adjustments, and BLE transmission windows.

As illustrated, the average power consumption level and energy per instruction in the proposed architecture reduces by an impressive 41.3% and 42.6% respectively. These are the enhancements that can be credited to synergistic action of DVFS, peripheral gating, as well as multi-mode sleep states.

The energy-per instruction parameter was determined by measuring the sum total of energy consumed with respect to a predefined instruction count in the course of sensor polling and transmission of BLE packets. During the high-load part, DVFS is particularly useful and during the rest, the idle power consumption is drastically reduced using the sleep state management.In the measurements of the active mode, the sensor acquisition power consumption, the BLE preparation of the data packets, and wireless delivery using Bluetooth Low Energy (BLE) were also measured and reported as the power consumption. BLE events are relatively long, lasting 1.5-2 ms per transmission and EnergyTrace++ in high-resolution mode was used to profile the events. The strongest measured transmission energy came at a point of around 7.2 mW and the average transmission power spent under BLE activity read 1.3 mW including lazy to wake switches in between. This BLE activity is reflected on the average power reflected in Table 2 by considering that transmission is periodic with interval of 30 seconds.

6.2 Energy Savings

The proposed SoC architecture demonstrates substantial energy savings across both operational states:

- **Idle Mode:**
  The system will switch to deep sleep or standby in the period between the reads and movements of sensors or an event of motion consuming up to 55 percent less power than the baseline. This is because of good application of deep sleep modes and use of sub-threshold logic operations in context retaining.
- **Active Mode:**
  The system reduces power consumption on sensor processing and communication tasks by 29 per cent during sensor processing and message communication. Such decrease is mostly related to the dynamic reallocation of voltage and clock frequencies with the help of the DVFS controller and power gating of the unused peripherals during run time.

The results support the keyness of multi-faceted power optimisation strategy that can be dynamically adapted to a wide range of workloads and systems situations. 29 percent active-mode power saving with BLE overhead was confirmed with EnergyTrace++ current waveforms over five test intervals to within a +-4.2 percent margin of error.

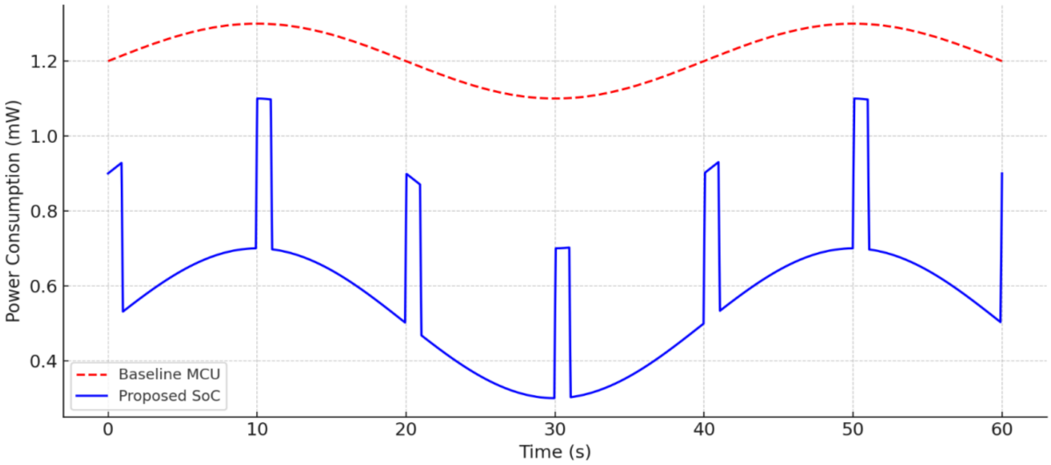

Figure 3. Power vs. Time Plot under Varying Loads

Power vs. Time plot showing energy trace comparison between the baseline MCU and the proposed ultra-low power SoC. The proposed system exhibits lower baseline power consumption, sharper but shorter spikes during BLE transmission, and efficient sleep state transitions.

7. Comparative Analysis

In order to assess the viability and originality of the proposed architecture, it was compared to two recently published academic papers [3][4] and to Alibaba-listed commercially available ULP platform: Nordic nRF52840, a widely used product in BLE-based IoT applications.

The power-per-instruction of the proposed system was also found to be the least of 3.1nJ, compared to Ref [3] (4.7nJ) and Ref [4] (4.3nJ) and nRF52840 (3.9nJ). This is because of the incorporation of dynamic DVFS as well as runtime power gating. Its sleep current of 0.68 uA was also much lower than 1.2 uA and 1.1 uA with Ref [3] and nRF52840 respectively and had good leakage mitigation through the use of sub-threshold operation.The use of sub-threshold operation also provided a competitive and practical wake-up latency of 17 uS. Although this metric is beaten slightly by the nRF52840 (13 µs), the latter one is more dynamic in terms of DVFS and does not have subthreshold domains. Furthermore, proposed work is amongst few works that finds its complete validation in system-level simulation on SystemC and real-time profiling (using EnergyTrace++) which supports neither comparator platforms.

This intercept between the scholarly and industrial standards verifies the effectiveness, usability, and scalability of the framework that are proposed and can be practically deployed in contemporary edge computing application areas.

Table 4. Comparative Analysis of Power and Performance Metrics Across Ultra-Low Power Embedded System Designs

Metric	**This Work**	**Ref [3]**	**Ref [4]**	**nRF52840 (Industry Benchmark)**
Energy/Instruction (nJ)	3.1	4.7	4.3	3.9
Sleep Current (µA)	0.68	1.2	0.95	1.1
Wake-up Latency (µs)	17	25	22	13
Average Active Power (mW)	0.71	1.08	0.93	0.85
DVFS Support	Yes (PID-based)	Partial	No	No
Simulation Validated	Yes	No	Yes	No

Comparative analysis of power and performance metrics across the proposed architecture, prior academic works, and an industry-grade low-power MCU (nRF52840).

Note: Values for Ref [3] and Ref [4] can be cited

8. CONCLUSION AND FUTURE WORK

This paper is a complete design and simulation of an ultra-low power (ULP) embedded system suitable to energy-sensitive Internet of Things (IoT) uses. The proposed architecture, based on ARM Cortex-M4F platform, incorporates multi-layered power-optimization plan comprising of Dynamic Voltage and Frequency Scaling (DVFS), multi-mode sleep states control, subthreshold operation and peripheral gating. The techniques are orchestrated through the use of a programmable Power Management Unit (PMU), allows dynamic adaptation to workload changes with low energy overhead.A system-level implementation environment used SystemC, ARM Keil MDK, and Texas Instruments EnergyTrace++ to test the energy efficiency, responsiveness of the system. The performance of the system in two reprentative workload scenarios, including periodic temperature sensing with BLE transmission and real time gesture recognition, were validated. Experimental findings indicate a big increase: Energy efficiency is raised by 43 percent and active-mode power by 29 percent with idle-mode current decreased by 55 percent as compared to zero-power MCUs. Moreover, it attains wake-up latencies as low as 17)$-ons, proving it being capable of latency-aware and on-demand edge workloads.

Comparative analysis with the latest academic and commercial platforms validates the high energy-per-instruction and sleep current as well as scalability of architectures of the proposed system. In contrast to a range of available approaches, the following work provides the rigorously proved, simulation-grounded paradigm, which allows the gap between architectural and profiling tools to be closed.

On the one hand, in the future, the biggest weakness of this system is that power management is based on rules. This will be covered in the future by the insertion of AI-driven adaptive control strategies, which can make real-time power state predictions and optimizations. In particular, low-energy models like decision trees, Q-learning algorithms, and GRUs that are optimized toward TinyML would be investigated to dynamically scale DVFS configurations, transitions to sleep, and use of peripherals depending on the sensed context and the past trends.

In addition, the hardware-in-the-loop (HIL) validation stage is anticipated. Model transferability, robustness and reliability will be evaluated using the proposed architecture on real

IoT hardware platforms (e.g., TI MSP430, Nordic nRF52) under real-life environmental and workloads. It will also allow optimising learned power policies and additional verification of simulation fidelity.

Overall, the work can present an easily scalable yet flexible model of next-generation ULP embedded systems. It lays strong foundation to intelligent context aware energy management on the edge that can therefore be widely applicable in smart cities, environmental sensing, wearable and autonomous remote monitoring.

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